9100FT/9105FT

Service Manual

P/N 910476
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FLUKE®

LIMITED WARRANTY

John Fluke Mfg. Co., Inc. (Fluke) warrants your 9100FT/9105FT to be free from defects in material and workmanship under normal use and service for one year from the date of shipment. The medium on which the 9100FT/9105FT software is furnished will be free from material defects and workmanship for 90 days from the date of shipment. Software and firmware products are provided “AS IS.” We do not warrant that software or firmware products will be error free, operate without interruption or that all errors will be corrected. This warranty extends to you if you are the original purchaser and does not apply to fuses, batteries, or any product which, in our sole opinion, has been subject to misuse, alteration or abnormal conditions of operation or handling.

To obtain warranty service, contact a Fluke Service Center or send the product, with the description of the difficulty, postage prepaid, to the nearest Fluke Service Center, Fluke assumes no risk for damage in transit.

Fluke will, at our option, repair or replace the defective product free of charge. However, if we determine that the failure was caused by misuse, alteration, or abnormal condition of operation or handling, you will be billed for the repair. The repaired product will be returned to you, transportation prepaid.

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INTRODUCTION 1-5.

The 9100FT/9105FT Service Manual provides overall service and maintenance information. It includes a comprehensive operational theory discussion, along with replacement parts lists and schematic diagrams. The Service Manual offers a detailed and technical description of the 9100FT and 9105FT and, when used with the 9100FT/9105FT Service Kit, can be used during troubleshooting procedures. This manual covers both standard mainframes and optional assemblies.

This Manual 1-6.

This manual documents issues encountered when servicing and repairing the 9100FT/9105FT. Other volumes of the 9100FT/9105FT manual set cover operating and programming the 9100FT and using the 9105FT. The 9100FT/9105FT Service Manual consists of the following sections:

Section 1: How to Use This Manual

This section introduces the Service Manual. It also defines some conventions used throughout the manual set.

Section 2: General Information

This section contains various types of often-used information. For quick reference, general descriptions of the instrument, its features, and its power requirements are given. Differences between the 9100FT and the 9105FT are mentioned. Test equipment called for in the rest of this manual is specified. Shipping and service procedures and addresses are also provided in this section.

Section 3: Theory of Operation

This section describes the 9100FT/9105FT in terms of major functional areas (termed blocks). Often, an individual functional block is further examined in terms of its own functional blocks. Where necessary, individual components are mentioned in describing the operation of a block and its relationship to other blocks. This information can be used with the schematic diagrams (found later in this manual) during troubleshooting.

Section 4: Maintenance

In addition to describing operator maintenance and adjustments, this section documents procedures required when disassembling, adjusting, or testing the 9100FT/9105FT. Section 4 also describes reassembly and interconnection of system units.

Section 5: List of Replaceable Parts

This section presents complete ordering information for any part that can be ordered separately. Federal Supply Codes and Manual Status Information are included here.

Section 6: Schematic Diagrams

This section contains schematic diagrams and reference designator drawings for each assembly (standard and optional) used in the 9100FT/9105FT.

The Manual Set 1-7.

Other manuals in the 9100FT/9105FT manual set are:

- Getting Started

  Describes functions and interconnections of the elements of a 9100FT or 9105FT system.

- Automated Operations Manual

  Describes the use of pre-programmed test or troubleshooting procedures.

- Technical User's Manual

  Describes the use of the 9100FT/9105FT keypad to test and troubleshoot a Unit Under Test (UUT).

- Applications Manual

  Describes how to design test and troubleshooting procedures for a Unit Under Test (UUT).

- Programmer's Manual

  Describes how to use a 9100FT programming station to create automated test and troubleshooting procedures.

- TL/1 Reference Manual

  A complete, alphabetical reference of the TL/1 programming language commands.

CONVENTIONS 1-8.

Throughout the manual set, certain notational conventions are used. A summary of these conventions follows:

- Instrument Reference

  Usually, a description applies to circuits found in both the 9100FT and the 9105FT. The instrument is then designated “9100FT/9105FT”. If a description applies to one instrument only, either “9100FT” or “9105FT” is used.

- Printed Circuit Assembly

  The term “pca” is used to represent a printed circuit assembly and its attached parts.

- Signal Logic Polarity

  Signal names followed by a “-” are active (or asserted) low. Signals not so marked are active high.

- Circuit Nodes

  Individual pins or connections on a component are specified with a dash (-) following the component reference designator. For example, pin 19 of U30 would be U30-19.

- Keystroke Notation

  The following conventions are used to identify syntax keystrokes and differentiate them from surrounding text:

(xxx)	When associated with a keyword, a lower-case word in parentheses indicates an input required by the user.
XXX	An uppercase word without parentheses indicates a literal keyword to be entered by the user.
<XXX>	Angle brackets around all upper-case letters means press the <XXX> key.

Section 2
General Information

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DESCRIPTION 2-1.

Information brought together in this section serves as a one-source reference for servicing the 9100FT, 9105FT, and related options. The 9100FT/9105FT instruments are fully described elsewhere in the manual set. Specifically, Getting Started and the Technical User's Manual can be consulted for hardware and capabilities information.

Power Requirements 2-2.

Power requirements for the 9100FT/9105FT are presented in Table 2-1. The 9100FT/9105FT mainframe uses a maximum of 150 watts. In addition, the Monitor uses 50 watts maximum.

External Connections 2-3.

Servicing the 9100FT/9105FT may require disconnection of system components. For ease of reassembly, full connection information is presented here. Figure 2-1 identifies connections and other features found along the right side of either instrument. Figure 2-2 shows rear panel features.

SYSTEM COMPONENTS 2-14.

Theories of operation, maintenance instructions, and schematic diagrams in this manual cover all 9100FT/9105FT system components. Refer to other manuals in the 9100FT/9105FT manual set for complete descriptions and usage instructions. The Getting Started manual provides a good overview of system components. These are listed and categorized in the following paragraphs, with references to coverage within this manual.

9100FT Systems 2-4.

The 9100FT Digital Test System constitutes the mainframe, probe, and clock module documented in this manual.

The 9100FT/SYS Digital Test Programming System includes 9100FT Test System components, along with the 9100A-003 Parallel I/O Module, the 9100FT-004 Programmer's Station, and the Y9100A-DCS DIP Clip Set accessory described in this manual.

9105FT System 2-5.

The 9105FT Test Station includes the mainframe, probe, and clock module described in this manual.

Options 2-6.

The 9100FT-004 Programmer's Station applies to the 9100FT only. Its monochrome monitor, monochrome video controller, and keyboard are documented in this manual.

The 9100FT-005 Programmer's Station is also available for the 9100FT only and provides the color video controller and keyboard described in this manual.

Table 2-1. Power Requirements

VOLTAGE SWITCH SETTING	LINE VOLTAGE RANGE	FREQUENCY	FUSE
110V	90-130V ac	47 to 440 Hz	2A Slow Blow
220V	180-264V ac	47 to 63 Hz	1A Slow Blow

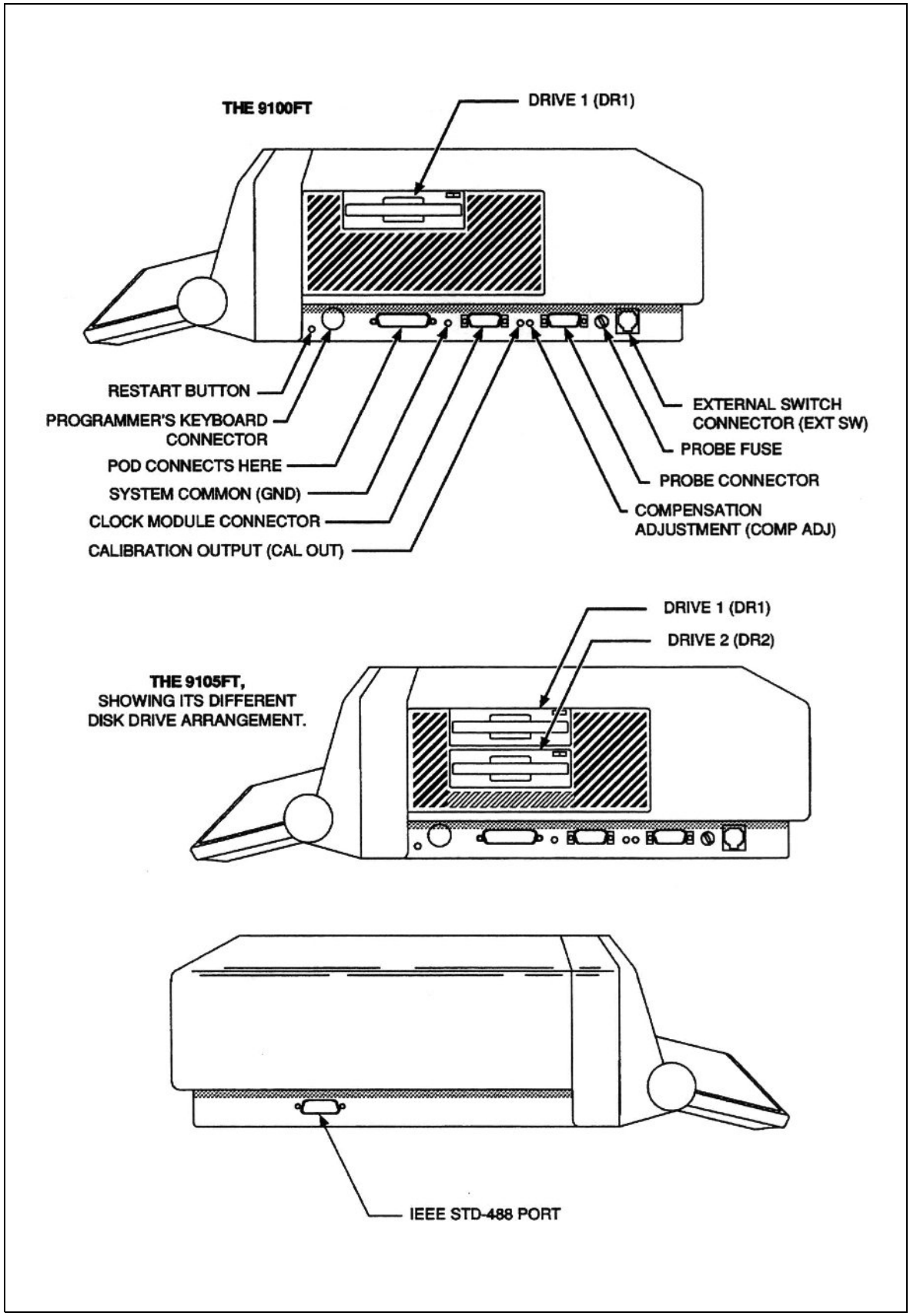

Figure 2-1. Side Features

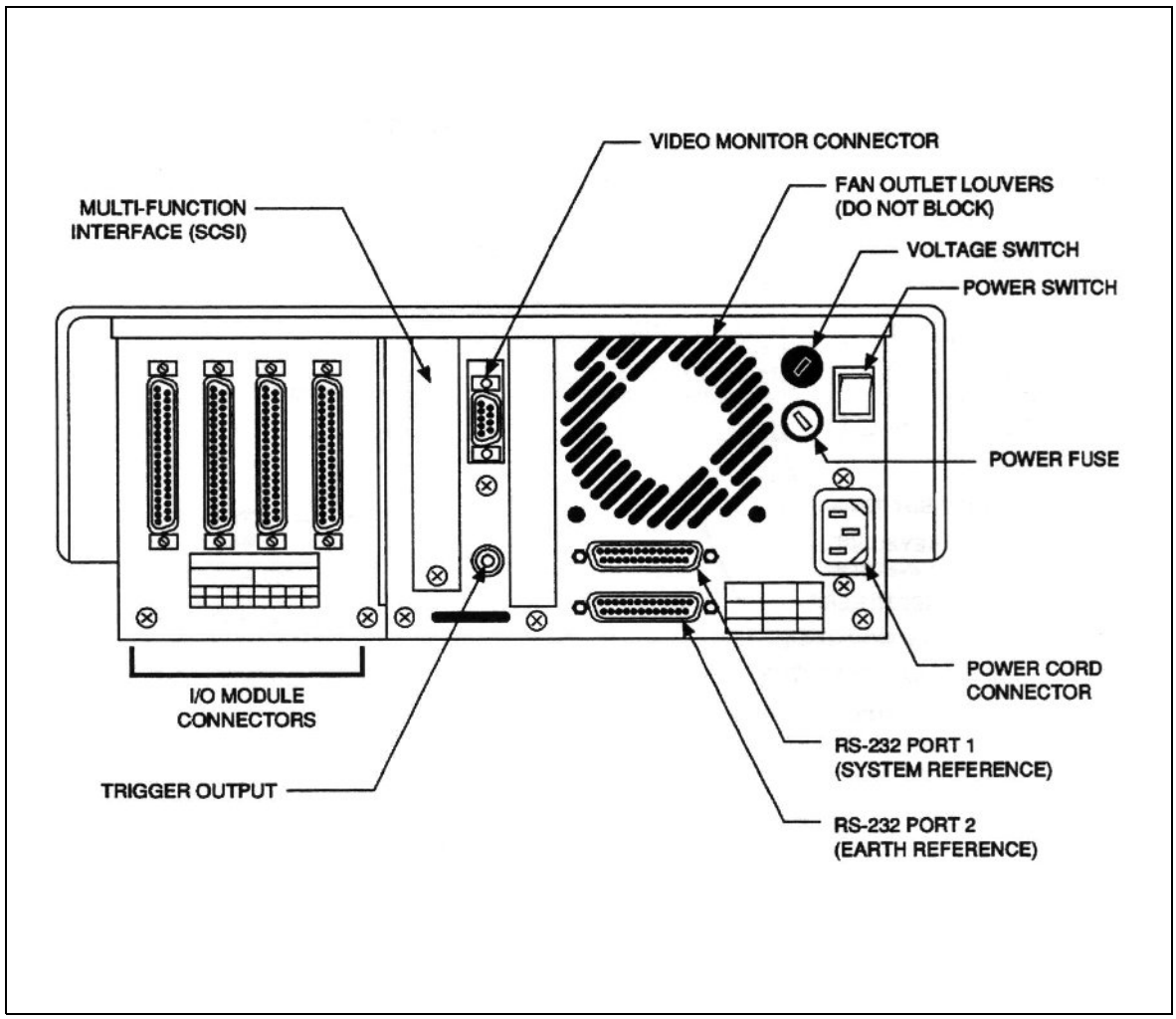

Figure 2-2. Rear Panel Features

The following options are available for either the 9100FT or the 9105FT and are separately documented in this manual:

- Parallel I/O Module, Option 9100A-003, includes a Y9100A-20L Flying Lead Module and a Calibration Module.
- Video (Monochrome), Option 9100A-009, includes a Video Controller and a Monochrome Monitor.
- Video Controller (Color), Option 9100A-011. Keyboard, Option 9100A-013

The Vector Output I/O Module, Option 9100A-017, is document in a separate manual (Fluke P/N 855531).

Accessories 2-7.

All hardware accessories for the 9100FT/9105FT are documented in this manual. These include:

- Half-Width Clip Modules, Accessories Y9100A-14D, -14S, -16D, -16S, -18D, 20D, 20S, -24D, and 24S.
- Full-Width Clip Modules, Accessories Y9100A-28D, -28S, and -40D.

- Y9100A-DCS DIP Clip Set, including Y9100A-14D, -16D, -18D, -20D, -24D, -28D, and -40D.
- Flying Lead Module, Accessory Y9100A-20L

Interface Pods 2-8.

Interface pods can be used with a wide range of microprocessors. Each pod is documented in its own manual, none of which are included with 9100FT/9105FT Manual Set. No pod information is provided in this service manual.

REQUIRED TEST EQUIPMENT 2-15.

Tools and test equipment required in servicing the 9100FT or 9105FT are listed in Table| 2-2.

SHIPPING INFORMATION 2-16.

When you receive the instrument, inspect the shipping container for any possible shipping damage. Special instructions for inspection and claims are included on the shipping container.

If it is necessary to reship the instrument, use the original container. If the original container is not available, a new one can be obtained from the John Fluke Manufacturing Co., Inc. upon request.

SERVICE INFORMATION 2-17.

The 9100FT/9105FT is warranted for a period of 1 year upon delivery to the original purchaser. The warranty is located in the front of this manual, following the title page.

Factory calibration and service for each Fluke product is available at various locations worldwide. A complete list of these service centers is given in the appendices of this manual. If requested, an estimate will be provided to the customer before any work is begun on an instrument whose warranty period has expired.

Maintenance plans are available to maintain the 9100FT/9105FT at your site, to supplement the normal warranty period, or to do both. For specific information, contact your nearest Fluke Technical Service Center or Sales Representative.

Table 2-2. Required Tools and Test Equipment

EQUIPMENT REQUIRED FOR GENERAL SERVICING		
EQUIPMENT	**RECOMMENDED MODEL**	**FUNCTION/COMMENTS**
Digital Multimeter	Fluke Model 77	
Oscilloscope	Philips Model PM 3065 (or equivalent)	
TTL Signal Source	Philips Model PM5193 (or equivalent)	
Power Supply		Variable, 0-5V, 0.5A min.
Resistors	20 Ohms (P/N 442202) 24 Ohms (P/N 442210) 33 Ohms (P/N 414524)	Switchable resistance box also acceptable.
Adjustment Tool	P/N 800540	
Video Terminal	CIT-101	
Null Modem Cable	Fluke Y1702	
IEEE-488 Controller	Fluke Model 1722A	
IEEE-488 Cable	Fluke Y8022	
Flat Blade Screwdrivers		1/8-inch (3 mm) blade 1/4-inch (6 mm) blade
Phillips Screwdriver		#2, blade 4 inches (10 cm) or longer
Hex Driver		3/16-inch (5 mm)
Hex Driver		5/16-inch (8 mm)
Wrench		3/16-inch (5 mm) or adjustable
REQUIRED EQUIPMENT FOR COMPONENT LEVEL REPAIR		
EQUIPMENT	**RECOMMENDED MODEL**	**FUNCTION/COMMENTS**
9100FT Service Kit	P/N 897116	
Digital Test Station, with I/O Module	Fluke 9105FT/9100FT with 9100A-003 Option	Runs programs supplied with Service Kit
Memory Interface Pod with 68030 Processor Support	Fluke Model 9132FT Fluke Model 9132FT-68030	Used with Service Kit
Surface Mount Service Kit	P/N 847855 (115V) P/N 847863 (230V)	For SMT repair

Table 2-2. Required Tools and Test Equipment (cont)

REQUIRED EQUIPMENT FOR MONOCHROME MONITOR MAINTENANCE		
EQUIPMENT	**RECOMMENDED MODEL**	**FUNCTION/COMMENTS**
Hex Adjustment Tool	P/N 572321	Horizontal Size/Linearity
Alignment Template	P/N 777144	Use with Monitor Pattern Program
Long-Nose Pliers		
Flat-Blade Screwdriver		1/4-inch (6 mm) blade, plastic handle with blade at least 5 inches (12.5 cm) long.
Phillips Screwdriver		#2, plastic handle with blade at least 3 inches (7.5 cm) long.
PhillipsScrewdriver		#2, non-magnetic tip blade, plastic handle, with blade at least 12 inches (30 cm) long, for CRT replacement.
Torque Hex Driver		3/16-inch (5 mm).
Soft Pad (foam or quilted)		Approximately 8 x 10 inches (20 x 25 cm).
1 Megohm, 1W Resistor	P/N 109793	To discharge CRT anode.
Clip Leads (2)		For connecting resistor to chassis and screwdriver shaft.
Safety Gloves		Mid-forearm length, soft leather.
Full Face Shield (preferred) or Safety Goggles		
Lab Smock with Zipper		Plastic zipper. Metal parts should not come in contact with the CRT.

SPECIFICATIONS 2-18.

Specifications for the 9100FT/9105FT are presented in Table 2-3.

Table 2-3. Specifications

ELECTRICAL SPECIFICATIONS

PROBE

Input Threshold

Logic Level	TTL Voltage	CMOS Voltage	RS-232 Voltage	ECL Voltage
1	2.6 to 5.0V	3.7 to 5.0V	3.2 to 30V	-1.15 to +30V
1 or X	2.2 to 2.6V	3.3 to 3.7V	2.8 to 3.2V	-1.35 to -1.15V
X	1.0 to 2.2V	1.2 to 3.3V	-2.8 to 2.8V	-
X or 0	0.6 to 1.0V	0.8 to 1.2V	-3.2 to -2.8V	-1.55 to -1.35V
0	0.0 to 0.6V	0.0 to 0.8V	-30 to -3.2V	-30 to -1.55V

Input Impedance . . . . . 70 kilohm shunted by less than 33 pF

Data Timing for Synchronous Measurements

Maximum frequency . . . . . 40 MHz

Minimum pulse width

High or low . . . . . 12.5 ns

3-state . . . . . 20.0 ns

Setup times

Data to Clock . . . . . 5 ns

Start, Stop, or Enable . . . . . 10 ns

to Clock

Hold time

Clock to Enable . . . . . 10 ns

Clock to Start or Stop . . . . . 0 ns

Data Timing for Asynchronous Measurements

Maximum frequency . . . . . 40 MHz

Minimum pulse width

High or low . . . . . 12.5 ns

Invalid (X)

TTL or CMOS. . . . . 100 ns ±20 ns

RS-232. . . . . 2000 ns ±400 ns

Transition Counting

Maximum frequency . . . . . at least 40 MHz

Maximum count . . . . . 16777215 (+overflow)

Maximum stop count . . . . . 65535 clocks

Frequency Measurement

Maximum frequency . . . . . at least 40 MHz

Resolution . . . . . 20 Hz

Accuracy. . . . . ±250 ppm or ±20 Hz, whichever is greater.

Table 2-3. Specifications (cont)

Output Pulser		
High	>3.5V @200 mA for less than 10 µs @ 1% duty cycle >4.0V @ 4 mA continuously	
Low	<0.8V @ 200 mA for less than 10 µs @ 1% duty cycle <0.4V @ 5 mA continuously	
CLOCK MODULE		
Input Thresholds (all lines)	1.6V ±0.2V	
Input Impedance	50 kilohm shunted by less than 10 pF	
Clock, Start, Stop, and Enable Input Speed		
Maximum repetition rate	40 MHz	
Minimum pulse width	12.5 ns	
RS-232 INTERFACES		
One connector isolated (system-referenced), the other connector non-isolated (earth-referenced).		
Baud rates	110, 134, 300, 600, 1200, 1800, 2400, 4800, 9600, 19200	
Parity	Odd, even, or none	
Data bits	5,6,7,or 8	
Stop bits	1,1.5,or 2	
XON/XOFF (Ctrl-S/Ctrl-Q)	Disable/Enable	
Clear-to-Send	Disable/Enable	
New line	Carriage Return and Line Feed (CRLF) or Carriage Return (CR)	
IEEE-488 INTERFACE		
Interface Function Subsets	SH1, AH1, T6, L4, SR1, RLO, PPO, DC1, DT1, C1, C2, C3, C4, C27, E2	
Mode	System Controller or Talker/Listener	
Primary Address	0-30	
Talker Terminator	<NONE>, <CR>, <LF>, <CR><LF>	
PARALLEL I/O MODULE		
Data Output, Static Operation		
Sourcing Current (total of all pins, all modules)	180 mA min	275 mA max
Sinking Current (total of all pins, all modules)	180 mA min	275 mA max
Data Output, Pattern Drive Operation (<10 ms)		
Sourcing Current (total of all pins, all modules)	1.8A min	2.75A max
Sinking Current (total of all pins, all modules)	1.8A min	2.75A max
Maximum sourcing current per pin (Vout >= 2.0V)	250 mA min	

Table 2-3. Specifications (cont)

Maximum sinking current . . . . . 150 mA min per pin (Vout <= 0.8V)

Maximum Pattern Depth. . . . . 255 patterns (one module driven)

Pattern Rate . . . . . Approximately 35 kHz (one module driven, 910XA)

I/O Module Input Thresholds

Logic Level	TTL Voltage	CMOS Voltage
1	2.6 to 5.0V	3.4 to 5.0V
1 or X	2.1 to 2.6V	2.9 to 3.4V
X	1.0 to 2.1V	1.2 to 2.9V
X or 0	0.6 to 1.0V	0.8 to 1.2V
0	0.0 to 0.6V	0.0 to 0.8V

Input Impedance . . . . . 50 kilohm minimum, shunted by less than 80 pF

Clock, Start, Stop, and Enable Inputs

Logic Thresholds

Low. . . . . 0.8V maximum

High . . . . . 2.0V minimum

Input Current . . . . . ±125 µA

Input/Output Overvoltage Protection . . . . . ±15V for one minute maximum, any pin, one at a time

Transition Counting

Maximum frequency. . . . . at least 10 MHz

Maximum count . . . . . 8388607 counts (+overflow) (transition mode)

Frequency accuracy. . . . . ±250 ppm or ±2 Hz whichever is greater (frequency mode)

Stop Counter

Maximum frequency. . . . . 10 MHz

Maximum count . . . . . 65535 clocks

Clock

Maximum frequency. . . . . 10 MHz

Minimum pulse width . . . . . 50 ns

Data Timing for Synchronous Measurements

Maximum frequency of clock . . . . . 10 MHz

Maximum frequency of data. . . . . 5 MHz

Data setup time . . . . . 30 ns

Data hold time . . . . . 30 ns

Minimum pulse width (data) . . . . . 75 ns

Minimum pulse width . . . . . 50 ns (Start, Stop, Enable, Clock)

Start edge setup time . . . . . 0 ns (before clock edge, for clock edge to be recognized)

Table 2-3. Specifications (cont)

Stop edge hold time	10 ns (after clock edge, for clock edge to be recognized)
Enable setup time	0 ns (before clock edge, for clock edge to be recognized)
Enable hold time	10 ns (after clock edge, for clock edge to be recognized)
Data Timing for Asynchronous Measurements	
Maximum frequency	10 MHz
Minimum pulse width (high or low)	50 ns
Minimum pulse width (3-state)	150 ns
Data Compare Equal (DCE)	
Minimum pulse width (Data and Enable)	75 ns
GENERAL SPECIFICATIONS	
Line Voltage	90 to 132V ac, 47 to 440 Hz 180 to 264V ac, 47 to 63 Hz
Power Consumption	
Mainframe	150W maximum
Monitor	50W maximum
Safety	
Designed to meet ANSI/UL 478, IEC 348, IEC 435, and CSA 556B standards.	
PHYSICAL SPECIFICATIONS	
Operating Temperature	
5°C to 27°C, 95% RH maximum (noncondensing) 27°C to 40°C, RH decreasing linearly from 95% to 50% (noncondensing)	
Programmer's Station	
24-line by 80-column CRT monitor with video controller installed in mainframe. 87-key keyboard with separate cursor control, and hardkey and softkey function keys.	
Storage/Shipping Temperature	
-20°C to 60°C, 8% to 80% RH (noncondensing). Micro-floppy media limited from 5°C to 60°C, 8% to 80% RH (noncondensing).	
Size	
Mainframe	14.0 x 34.3 x 50.8 cm (H x W x D) (5.5 x 13.5 x 20.0 in)
Monitor	30.5 x 33.5 x 33.0 cm (H x W x D) (12.0 x 13.2 x 13.0 in)
ASCII Keyboard	5.1 x 21.1 x 47.2cm (H x W x D) (2.0 x 8.3 x 18.6)
Weight	
Mainframe	8.3 kg (18.2 lb)
Monitor	11.1 kg (24.5 lb)
ASCII Keyboard	1.6 kg (3.5 lb)

Section 3
Theory of Operation

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OVERVIEW 3-1.

This overview of the Fluke 9100FT/9105FT explains the general relationships of the unit blocks contained in the 9100FT Block Diagram, Figure 3-1, and the 9105FT Block Diagram, Figure 3-2. Wherever a block performs the same function for both instruments, an identical block name is used for ease of reference later in this section.

Main PCA 3-2.

The Main Printed Circuit Assembly contains the following functional blocks:

- 68030 Microprocessor
- Read/Write (RAM) Memory
- Read-Only (ROM) Memory
- Floppy Disk Drive Controller
- Pod Interface
- Power Supplies for the RS-232 ports, operator's display, and video.

The Main PCA contains the interfaces for expansion cards, serial ports, the Operator Keypad, and the Programmer's Keyboard. There are connections for the Operator's Display, the Floppy Disk Drive, the Monitor, the Hard Disk Controller, the Probe I/O-ECL PCA, the microprocessor Interface Pod, and the switching Power Supply.

RS-232 Ports 3-3.

Two RS-232-C serial ports are available on the 9100FT. These ports allow data transfer to and from the tester. One is system-referenced (isolated from earth) and is used with the UUT. The other is a non-isolated port and is used for connection to another tester, computer, or printer. The Serial Port connectors are located at the rear of the Chassis.

Micro Floppy Disk System 3-4.

The Floppy Disk System uses 3.5-inch double-sided, double or high density disks. A disk has a formatted capacity of either 640K or 1.2M bytes. The 9100FT uses one disk drive, and the 9105FT uses two disk drives. The floppy drive is connected through J9 on the Main PCA.

Hard Disk System 3-5.

The 9100FT contains a 40M byte, 3.5-inch Hard Disk to store the operating software, user programs, and data. The Hard Disk interfaces to the Multi-Function Interface (MFI) II PCA, which implements the SCSI interface standard. The MFI II PCA, which plugs into the Main PCA at J11, also includes the non-volatile real-time clock, the DMA circuitry, and the IEEE-488 interface.

Power Supply 3-6.

The Power Supply for the 9100FT/9105FT is an OEM (original equipment manufacturer) switching power supply. Input voltage is switchable for either 90 to 132V ac or 180 to 264V ac operation. This functional block supplies one +5V, one -5V, and two +12V outputs to the system.

Operator’s Display 3-7.

The Operator’s Display is a vacuum-fluorescent display, 254 pixels wide by 26 pixels deep, allowing for 3 lines of 42 characters each. The Display is located above the Operator’s Keypad on the mainframe. The Display Interface PCA is connected to J10 on the Main PCA.

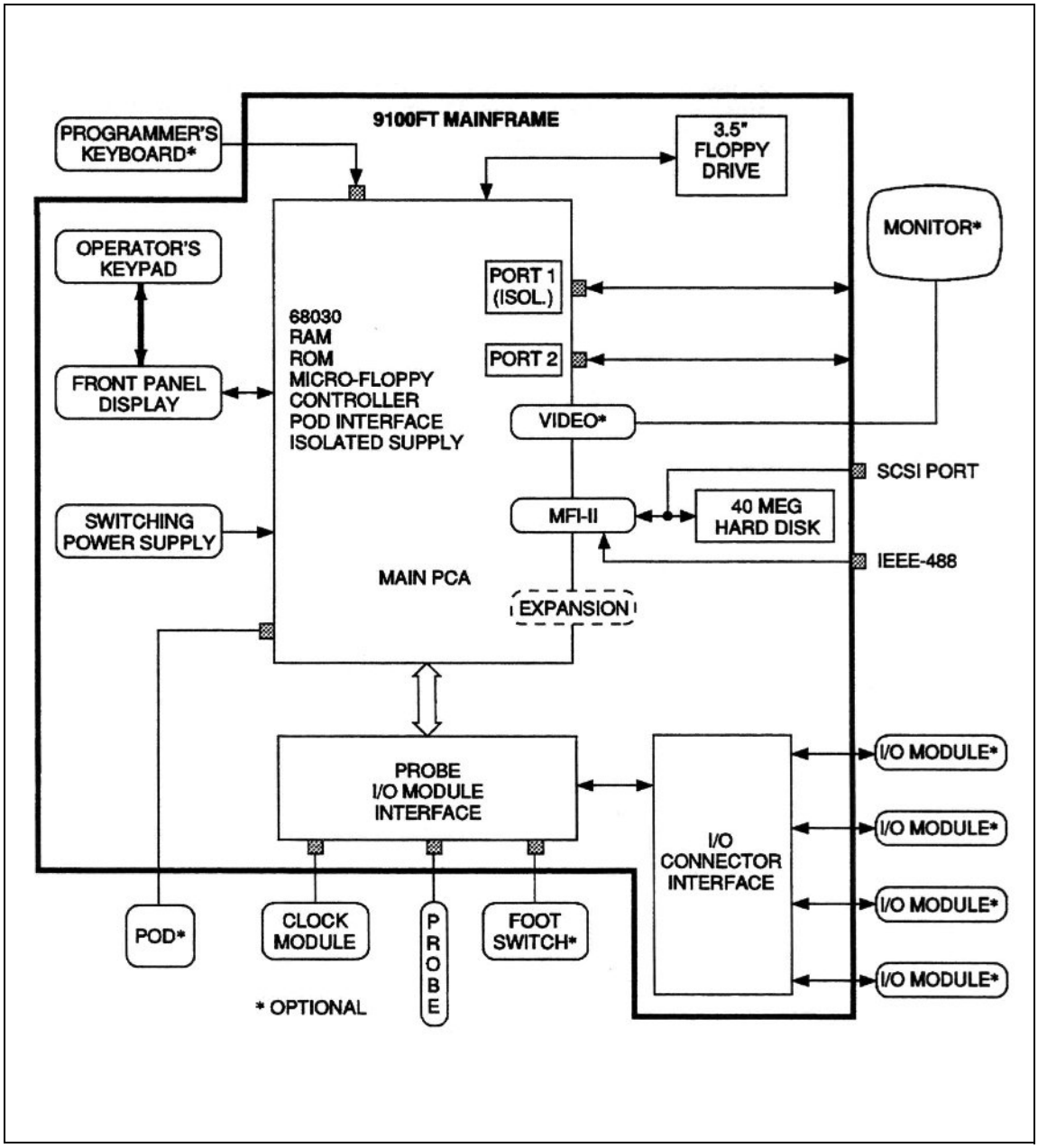


Figure 3-1. 9100FT Block Diagram

Operator's Keypad 3-8.

The Operator's Keypad is a part of the mainframe unit that, when folded down, faces the operator. It is connected to J2 on the Display Interface PCA. It contains all of the keys needed by the operator to run pre-programmed tests used in the immediate troubleshooting mode.

Probe/Pulser 3-9.

The Probe is a single-point, hand-held instrument that can measure signals up to 40 MHz. The Probe also acts as a pulser. The Probe is useful for circuitry that cannot be accessed with the I/O Module or Interface Pod. The Probe plugs into a connector on the side of the Chassis (J1 on the Probe I/O-ECL PCA.)

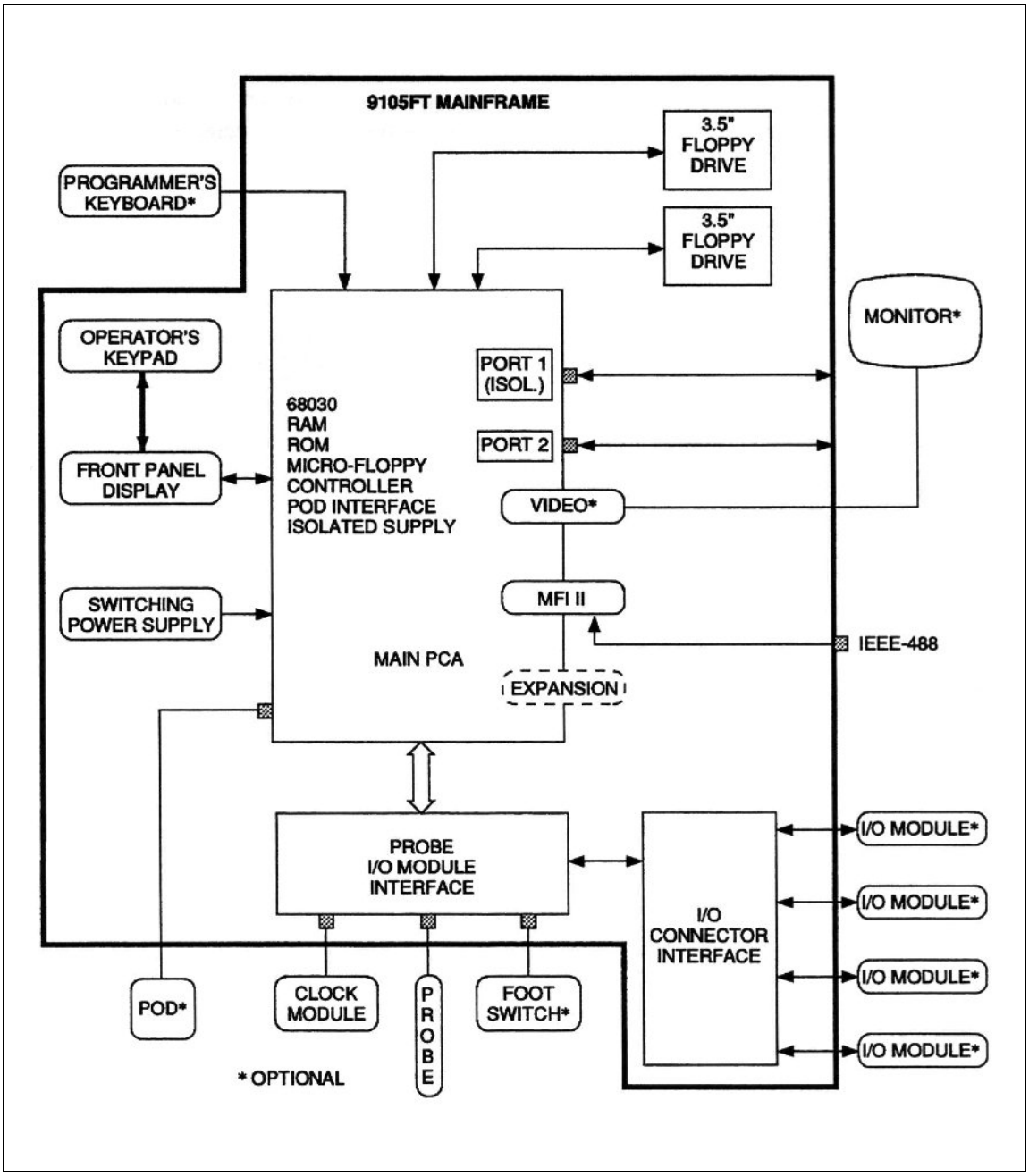


Figure 3-2. 9105FT Block Diagram

Clock Module 3-10.

The Clock Module is an external unit connected to the mainframe through J3 on the Probe I/O-ECL PCA. The Clock Module provides connections to external clock signals for troubleshooting signals asynchronous to the UUT microprocessor.

Monitor 3-11.

The Monitor displays programming information entered from the Programmer's Keyboard. The Monitor can also assume Operator Keypad functions by displaying procedural information. The Monitor is connected to a Video Controller Card, which is plugged into the Main PCA.

Programmer's Keyboard 3-12.

The Programmer's Keyboard is used for program development. It is also available as an option for data input to user programs. The Keyboard is connected to J15 on the Main PCA.

Parallel I/O Module 3-13.

NOTE

For information on the Vector Output I/O Module (Option -017), refer to the separate Vector Output I/O Module Service Manual (P/N 855531).

The Parallel I/O Module (9100A-003) is an external unit used for data stimulus and response of up to 40 channels at one time. An assortment of clip modules is available for interface to the UUT. The 9100FT can accommodate four I/O Modules at once, allowing for testing of 160 pins at a time. The 9100FT has the capability to take CRC (cyclic redundancy check) signatures, measure frequency, take event counts, record logic levels, and drive output patterns on each pin. The I/O Modules plug into the I/O Connector PCA, which plugs into the Probe I/O-ECL PCA.

MAIN PCA (68030 MICROPROCESSOR) DETAILED CIRCUIT DESCRIPTION 3-14.

Overview 3-15.

The 9100FT/9105FT uses a 68030 main processor. The 32-bit 68030 contains 17 32-bit registers (8 data registers, 7 address registers, and 2 registers used as stack pointers.) A 16-bit status register and a 32-bit program counter are also included. The 68030 (U40) is located on the Main PCA of the mainframe. For further information on the 68030 signals and operation, consult the 9132FT 68030 Pod Manual. Address ranges are identified in Table 3-1. A pin description is shown in Figure 3-3 and Table 3-2.

Table 3-1. 68030 Address Ranges

HEX ADDRESS	USE
000000 - 07FFFF	ROM
080000 - 08FFFF	Floppy Control
090000 - 093FFF	DTIO #1: Keypad/Display, RS-232 Port #2 DTIO #2: ASCII Keyboard, RS-232 Port #1
094000 - 097FFF	Interrupt Vector (Read)
098000 - 09BFFF	Parity Latch
09C000 - 09FFFF	Pod Interface
0A0000 - 0AFFFF	Expansion Card Slot
0B0000 - 0BFFFF	Multi-Function Interface II Card Slot
0C0000 - 0CFFFF	Logic Probe Circuitry
0D0000 - 0DFFFF	I/O Modules
0E0000 - 0EFFFF	Video RAM
0F0000 - 0FFFFF	Video Controller Chip
100000 - FFFFFF	RAM

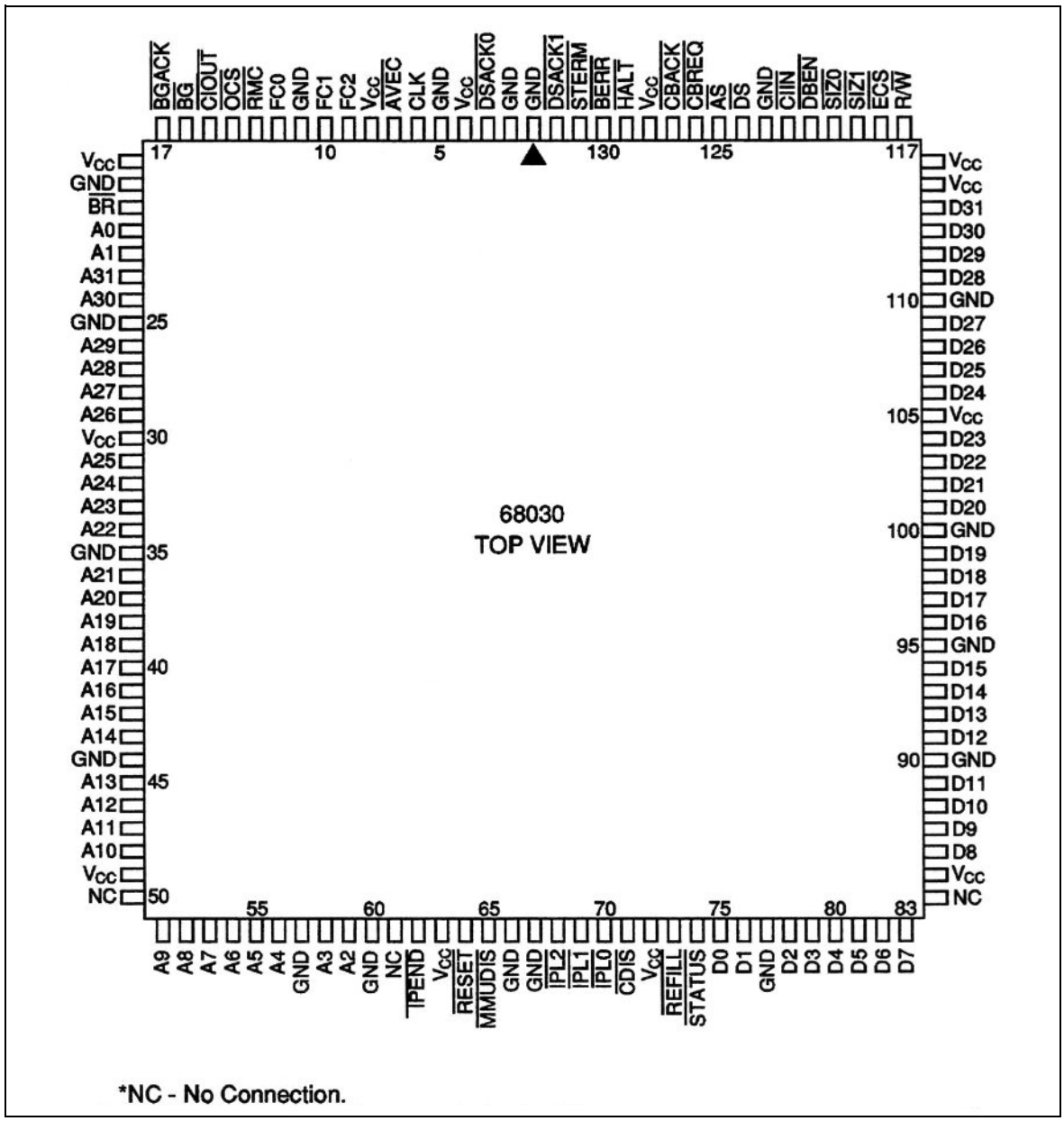


Figure 3-3. 68030 Pin Assignments

INTERRUPTS 3-16.

The 9100FT/9105FT system uses 15 different interrupts, allowing hardware and software to control 68030 operation and identify an error or specific condition. The interrupts are prioritized by importance as follows:

- The Parity Error Interrupt (I15) is level 7, which is non-maskable (NMI).
- All level 6 and lower levels are software maskable by level.
- Levels 7 through 2 are each used by only one interrupt.
- The level 1 interrupt is shared by several different interrupts. The interrupts within level 1 have priorities to prevent simultaneous requests.
- Level 0 indicates no interrupt is pending.

Table 3-2. 68030 Pin Locations

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
21	A0	7	AVEC-	103	D22	100	GND
22	A1	130	BERR-	104	D23	110	GND
59	A2	16	BG-	106	D24	123	GND
58	A3	17	BGACK-	107	D25	129	HALT-
56	A4	20	BR-	108	D26	62	IPEND-
55	A5	127	CBACK-	109	D27	70	IPL0-
54	A6	126	CBREQ-	111	D28	69	IPL1-
53	A7	71	CDIS-	112	D29	68	IPL2-
52	A8	122	CIIN-	113	D30	65	MMUDIS-
51	A9	15	CIOUT-	114	D31	50	NC
48	A10	6	CLK	121	DBEN-	61	NC
47	A11	75	DO	124	DS-	84	NC
46	A12	76	D1	3	DSACK0-	14	OCS-
45	A13	78	D2	132	DSACK1-	73	REFILL-
43	A14	79	D3	118	ECS-	64	RESET-
42	A15	80	D4	12	FC0	13	RMC-
41	A16	81	D5	10	FC1	117	R/W-
40	A17	82	D6	9	FC2	120	SIZ0
39	A18	83	D7	1	GND	119	SIZ1
38	A19	86	D8	2	GND	74	STATUS-
37	A20	87	D9	5	GND	131	STERM-
36	A21	88	D10	11	GND	4	VCC
34	A22	89	D11	19	GND	8	VCC
33	A23	91	D12	25	GND	18	VCC
32	A24	92	D13	35	GND	30	VCC
31	A25	93	D14	44	GND	49	VCC
29	A26	94	D15	57	GND	63	VCC
28	A27	96	D16	60	GND	72	VCC
27	A28	97	D17	66	GND	85	VCC
26	A29	98	D18	67	GND	105	VCC
24	A30	99	D19	77	GND	115	VCC
23	A31	101	D20	90	GND	116	VCC
125	AS-	102	D21	95	GND	128	VCC

Pending interrupts are detected between instructions. An interrupt is acknowledged and the service routine is started only if the pending interrupt has a higher priority than the current processor priority. When an interrupt is acknowledged, the hardware places a vector value on the data bus. This vector points to the memory location where the address of the interrupt routine is stored. An interrupt request must be reset by the interrupt acknowledging routine. Individual interrupt descriptions in the following paragraphs provide more details.

A list of hardware generated exceptions and their vectors is shown in Table 3-3. These exception vectors are listed by priority, with the top priority vector listed first. The maximum number of vectors is 256. The vectors with priority levels 1 through 7 (refer to

Table 3-3) are hardware generated during an interrupt acknowledge. Bus Error and Reset behave differently, always going to a predetermined address.

Most of the interrupt priority logic is included in LCA (Logic Cell Array) U25. Whenever an interrupt becomes active, the LCA prioritizes all interrupts, honoring the highest priority interrupt first. The interrupt request is pipelined with an internal 12.5-MHz clock, which is disabled while address strobe is active. The highest priority interrupt is the parity error interrupt, and the lowest priority is the self-vectored interrupt. The correct priority is assigned to the interrupt control signals (IPL0, IPL1, and IPL2). When an interrupt acknowledge cycle occurs, the LCA provides both the correct interrupt vector to the data bus and the terminating signal (DSACK0-).

During an IO or self-vectored interrupt, LCA U25 sends an interrupt acknowledge to the interrupting device through either the Multi-Function Interface II PCA (MCINTA-) or the Expansion PCA (ECINTA-). The interrupting device can then supply the DTACK- and the vector. The LCA contains the arbitration circuitry for the interrupts and interrupt acknowledge of the MFI II and expansion assemblies to return the correct interrupt acknowledge to the device generating the interrupt.

Parity Error Interrupt 3-17.

The 9100FT/9105FT checks parity on RAM reads. The 68030 reads all four bytes during a RAM access. Therefore, parity is checked for the full 32-bit word, although each byte is treated separately by the parity system. When a parity error is detected, the non-maskable Parity Error Interrupt (I15) is set, and the SIMM (Single Inline Memory Module) location of the error is latched. The latch is byte readable at address 098002 and is described in Table 3-4.

Table 3-3. Interrupt Vector Table

LEVEL	NUMBER	NAME	HEX VECTOR	HEX ADDRESS
*	RESET	Reset	00	00000
*	BERR	Bus Error	02	00008
7	I15	Parity Error Interrupt	8F	0023C
6	I14	Floppy Data Interrupt	9F	0027C
5	I13	DTIO # 1 Interrupt	AF	002BC
4	I12	DTIO # 2 Interrupt	BF	002FC
3	I11	MFI Card Interrupt 2	CF	0033C
2	I10	Expansion Card Interrupt 2	DF	0037C
1	I9	Floppy Controller Interrupt	EF	003BC
-	I8	Not Usable		
1	I7	Probe Interrupt	78	001E0
1	I6	I/O Over-Current Interrupt	79	001E4
1	I3	I/O Module General Interrupt	7C	001F0
1	I2	I/O Module DCE Interrupt	7D	001F4
1	I0	Self-Vectored Interrupt		
-	--	No Interrupt	77	001DC

Table 3-4. Microprocessor Parity Status Latch @ 98002

BIT #	7	6	5	4	3	2 1 0
NAME	BITS 24-31	BITS 16-23	BITS 8-15	BITS 0-7	BANK 0-1	
• Bits 4-7 are set if the parity error occurred in that bank of RAM. • Bit 3 is set if the parity error occurred in BANK 1 (U38, U43, U50, U52) else the error occurred in BANK 0 (U35, U37, U48, U51).						

Floppy Data Interrupt 3-18.

The Floppy Data Interrupt is generated by the floppy controller when it either needs the next byte of data while doing a write or when the next byte of data is available in read mode. The interrupt is automatically cleared when the byte is received or read. The interrupt can be enabled or disabled by a bit in the floppy controller latch. It can be individually polled at DTIO #2 Input Port, bit 4.

DTIO #1 Interrupt 3-19.

The DTIO #1 Interrupt is generated by the DTIO (Dual UART/Timer/IO) #1 in response to a variety of conditions that may include the following:

- Transmit Buffer Empty
- Receive Buffer Full
- Break Received
- Timer Interrupt
- Pod Change
- 500 millisecond (Frequency Gate)

All possible interrupts can be polled at the ISR (Interrupt Status Register) of the DTIO. A separate register, the IMR (Interrupt Mask Register), is used to program which of the possible interrupts is allowed to generate an interrupt. After an interrupt is generated, the ISR must be read to determine the cause. Different actions are needed to reset the different types of interrupts.

DTIO #2 Interrupt 3-20.

The DTIO #2 Interrupt is generated by the second DTIO and is similar in function to the DTIO #1 Interrupt. Possible DTIO #2 conditions include:

- Transmit Buffer Empty
- Receive Buffer Full
- Break Received
- Timer Interrupt
- Disk Change

MFI Card Interrupt 2 3-21.

This interrupt is generated by a peripheral on a card plugged into the Multi-Function Interface (MFI) II Card Slot. The MFI Card Interrupt 2 is intended to be used by the SCSI controller chip under program control. This interrupt can be software disabled and polled. The MFI Card Interrupt 2 is not used on the 9105FT.

Expansion Card Interrupt 2 3-22.

The Expansion Card Interrupt 2 is reserved for devices connected to the expansion bus.

Floppy Controller Interrupt 3-23.

The Floppy Controller Interrupt is generated by the floppy controller in response to a variety of conditions. The interrupt status register of the chip must first be read to determine the cause for the interrupt. The interrupt can be individually polled at DTIO #2 Input Port, bit 5.

Probe Interrupt 3-24.

The Probe Interrupt is generated by the single-point probe for either a blown fuse or a button press. A probe chip status register read is performed to determine the cause.

I/O Over-Current Interrupt 3-25.

The Parallel I/O Module power supply generates an over-current interrupt (IOOCI) when the current limit is exceeded. The interrupt is generated and latched on the Probe I/O-ECL PCA, located in the mainframe. If this interrupt should occur, a control signal (ODRESET-) is sent to the Parallel I/O Module, which instantly turns off the overdrivers. Before clearing the interrupt, the overdrivers must be written to the tristate condition.

I/O Module General Interrupt 3-26.

This interrupt can be caused by a button press on an I/O Module. The interrupt status register(s) on the I/O Module(s) must be read to determine whether the left or right clip module button was pushed.

I/O Module Data Compare Equal Interrupt 3-27.

The I/O Module Data Compare Equal Interrupt is generated by one of the I/O Modules when the programmed data compare register matches the input data.

Self-Vectored Interrupt 3-28.

The Self-Vectored Interrupt (IO) is a special case. It can be generated by more than one device in either the MFI II PCA Slot or the Expansion Bus PCA Slot. A separate Interrupt Acknowledge (INTA) is sent to each pea slot to indicate which interrupt is being acknowledged. When acknowledged, the initiating device must supply a vector and a DTACK- or a VPA- (for auto-vectoring mode).

No Interrupt 3-29.

This vector is read if no interrupts are pending or if the interrupting device removed the request before the interrupt acknowledge cycle.

Asynchronous Execution 3-30.

The 68030 can operate independently of the clock frequency by using only the handshake lines (AS-, DSACK0-, DSACK1-, DS-, STERM-, BERR-, HALT-) for data transfer control. The AS- signal is issued by the microprocessor to begin the bus cycle. The data strobe signals verify that the data is valid on a write cycle. The memory space (or peripheral) either places the requested data on the bus for a read cycle or latches the data on a write cycle. The DTACK- signal is issued by the data source to end the bus cycle and is turned into DSACK0- or DSACK1- by LCA U25, depending on the responding port width. If there is no response from the data source or if a wrong address is accessed, BERR- is sent to the 68030 to abort the bus cycle. The Dynamic RAM subsystem always returns DTACK-; it never generates a bus error, even for Dynamic RAM accesses to aliased memory.

Reset Signal 3-31.

There are four sources for the Reset signal:

- Power-Up Reset

  This is a “cold” start. It occurs at power up, allowing the processor to initialize the system.

- External Reset

  The hardware has an external switch that allows the user to reset the system. This reset button is debounced by circuitry on the reset chip.

- Power Glitch Reset

  The mainframe detects when the 5V dc supply falls below 4.5V dc, then asserts a reset pulse for approximately 250 ms.

- Watchdog Reset

  If watchdog mode is selected (by closing dip switch S1-7), any pause longer than 1.2 seconds in accessing the UART that generates the time slice interrupt results in a system reset. The default condition is watchdog mode disabled.

The reset circuitry located on the Main PCA consists of a specialized reset chip (U49) that contains a power supply voltage window comparator, a debounce circuit for an external reset switch (S2), a watchdog timer, and a reset pulse generator.

Address Decoding and DTACK 3-32.

Address decoding is accomplished in two different stages for the ROM and Dynamic RAM and for the remaining peripherals. U32 decodes the memory space into either ROM and I/O or RAM and controls the enabling of the Dynamic RAM controller. Any address higher than the first 1M byte of the address space is considered Dynamic RAM (except when an interrupt acknowledge is in progress.) During an interrupt acknowledge, addresses are in the range FFFFFFFx, where ‘x’ is the interrupt level being serviced. Address line A31 is high only during these cycles and is used to disable the RAM while the vector register is being read.

For addresses in the lower 1M byte of the address space, the line ‘ROM/IO-’ is asserted by U32 and used by LCA U25 to further decode the addresses for the ROM and the peripherals. All remaining address space is allocated to RAM. The various RAM spaces used depend on the type and quantity of Dynamic RAM SIMMs inserted, as shown in Table 3-5.

The various RAM configurations require setting of bank select switches S1 5 and 6, as follows:

Table 3-5. RAM Space

SIMM TYPE	SIMM QUANTITY	RAM SPACE USED	RAM TOTAL
1M byte	4	100000-4FFFFF	4M bytes
1M byte	8	100000-8FFFFF	8M bytes
4M byte	4	100000-FFFFFF	15M bytes
When 4M byte SIMMs are used, 1M byte of RAM is lost to the I/O mapping.			

- If one bank of RAM is inserted, switch 6 is closed and switch 5 is open.
- If two banks of RAM are installed, switch 5 is closed and switch 6 is open.

The actual RAM present is determined by using aliasing tests during the boot-up procedures.

The assertion of the processor DSACK0- and DSACK1- bus control signals is provided by the DTACK section of the LCA. It is divided into two separate state machines for bus cycles terminated by an external DTACK- signal from the I/O bus and for bus cycles terminated internally by the LCA. Since the I/O bus is treated as a 16-bit port by the 68030, all DTACKs originating on the I/O bus are converted to a DSACK1 control signal. The external DTACK signal is delayed two clock cycles before DSACK1 is asserted for two clock cycles, guaranteeing recognition and assuring that DSACK1 is inactive before the next address strobe goes active (in spite of the delays through the LCA.)

The internal DTACK is generated for accesses to the ROM, the floppy, the parity status register, the Probe I/O-ECL PCA, and the interrupt status register. All addresses (except the ROM and interrupt status register) generate a DSACK1 that indicates a 16-bit port. The ROM and interrupt status register addresses generate a DSACK0 to indicate an 8-bit port.

Either internal DTACK is generated on the 14th clock after the start of the bus cycle and is asserted for two clock cycles. The state machine controlling the DTACK also generates the special data strobe (NDSWR-) for the floppy controller chip to ensure adequate set-up and hold time during writes to this very slow chip. Internally generated DTACK is timed for the worst case access time of the chips it controls, which in this case is the floppy controller chip on the Main PCA.

A further divide-by-eight following the internal DTACK counter asserts the bus error signal after 128 clocks have transpired without an external DTACK.

Bus Arbitration 3-33.

The two I/O bus requests (MCINT1- and ECINT1-) are sampled by input flip-flops in LCA U25, which are driven by a 12.5-MHz clock. If either request is active, the processor bus request is driven on the next clock. The first request to become active sets the R-S arbitration flip-flop and asserts the individual I/O bus grant on the next clock. The assertion of bus grant acknowledge (BGACK-) latches the winning requester. The release of bus grant by the processor resets the individual bus grant to the I/O bus. A new bus master arbitration is allowed as soon as the new bus master has released the bus by deasserting BGACK-.

The new bus master address strobe is synchronized inside U25 to the system clock. Assertion of AS- is delayed until at least one of the CAS enable lines (LLOUT-, LMOUT-, UMOUT-, UUOUT-) has gone active, ensuring that the Dynamic RAM controller has a stable CAS line enable before starting the access. A state machine in LCA U25 prevents any glitching on the AS- line, which could cause the internal state machine in the Dynamic RAM controller to fail. The state machine in U25 generates an internal AS- that goes active at the falling edge of the I/O bus AS- and is driven inactive only after all data strobes have been released by the bus master.

The DTACK control logic in LCA U25 stretches the STERM signal from the Dynamic RAM controller until AS- goes inactive, allowing time for the slow bus master to respond to the DTACK- signal.

During a bus master operation, the state of A1 determines selection of the high word or low word data buffer between the processor/Dynamic RAM controller data bus and the I/O data bus.

Data Strobe Generation 3-34.

The LDS- and UDS- data strobes on the I/O bus are generated from a combination of the processor DS-, the decoded size lines from PAL U32, and the timing strobes generated from the DTACK logic. The lines are only asserted when the processor has control of the bus. During a bus grant cycle, these lines are monitored to generate the CAS enable lines for the Dynamic RAM controller.

E Clock, DC/DC Converter Clock Generation 3-35.

A divide-by-16 counter lowers the system clock to 1.56 MHz for use by the I/O bus. Further division by 3 and 16 generates the 33-kHz, non-overlapping, push-pull clock to the DC/DC Converter.

RAM Configuration 3-36.

Standard RAM configuration is 4M bytes of RAM for both the 9100FT and the 9105FT. Either instrument can be expanded to 15M bytes of RAM. Dynamic RAM access time is 80 ns; Dynamic RAM must offer a fast page mode. A DIP switch (S1) must be set for each RAM configuration. The settings are shown in Table 3-6.

Dynamic RAM Controller 3-37.

The Dynamic RAM is selected by PAL U32 when the processor addresses range 100000-FFFFFF. The ROM/IO- line from the PAL is active in the address range 000000-OFFFFF. All addresses are truncated to 24 bits to be compatible with the I/O bus, but address line A31 is monitored to indicate when an interrupt cycle is in progress in order to disable the Dynamic RAM. The RAM- line is active whenever AS- is active and the address is in the range of the Dynamic RAM. The ADS- line goes active after RAM- goes active on the first high system clock to avoid violating the set-up and hold time of the DTACK- state machine inside the Dynamic RAM controller. ADS- goes inactive immediately on AS- going inactive.

Page mode operation of the Dynamic RAMs is supported and results in two-cycle memory reads during cache fill burst operations. The incrementing CAS addresses are supplied by PAL U31 during burst accesses and is enabled by an active CBREQ- signal from the processor. All Dynamic RAM accesses from the I/O bus and all write operations from the processor are standard five-cycle single accesses.

Table 3-6. RAM Configuration

RAM COMPLEMENT	TOTAL BYTES	ADDRESS RANGE	SWITCH SEGMENTS 1234 5678
1 BANK of 1M Byte SIMM	4M	100000-4FFFFF	XXXX 01XX
2 BANKS of 1M Byte SIMM	8M	100000-8FFFFF	XXXX 10XX
1 BANK of 4M Byte SIMM	15M	100000-EFFFFF	XXXX 01XX
			1 = ON (closed) 0 = OFF (open)

Dynamic RAM refresh is provided by the Dynamic RAM controller and occurs at approximately a 12-us rate. Refresh is disabled during slow DMA accesses from the I/O bus. Refresh requests are thereby accumulated during longer DMA accesses.

The Dynamic RAM controller is configured during the first write to RAM after system reset. The mode line input to the controller is driven active during reset and held by PAL U31 until the first write to RAM. Holding the mode line active prevents the chip from randomly asserting the RAS and CAS lines before being configured. The rising edge of the mode line latches in the address, ECAS0-3, and B1 lines; this information is used as configuration data. A word write to address 8372B700 results in the configura- tion shown in Table 3-7.

Table 3-7. DRAM Controller Configuration

BIT	ADDR	VALUE	DESCRIPTION
B0	A25	1	Transparent address latch, no column increment
B1	A22/A24	1	asynchronous access
ECAS0	LL-	0	select WE-
ECAS1	LM-	1	68030 page burst mode
ECAS2	UM-	1	68030 page burst mode
ECAS3	UU-	0	68030 page burst mode
R0	A12	1	RAS- asserted 3T during refresh
R1	A13	1	RAS- precharge 3T
R2	A14	0	DTACK- 2T (3 wait states) during opening access
R3	A15	1	DTACK- 2T
R4	A16	0	DTACK- 1T (1 wait state) during burst
R5	A17	1	DTACK- 1T
R6	A18	0	increment address when CAS negated
R7	A19	0	DTACK rising edge triggered
R8	A20	1	non-interleaved
R9	A21	1	staggered refresh
C0	A2	0	rfclk/10
C1	A3	0	rfclk/10
C2	A4	0	rfclk/10
C3	A5	0	internal rfclk/30
C4	A6	0	2 RAS/byte
C5	A7	0	2 RAS/byte
C6	A8	1	2 RAS/byte
C7	A9	1	0 ns tASC
C8	A10	1	12ns tRAH
C9	A11	0	don't delay CAS during write

A31 - A24	A23 - A16	A15 - A8	A7-AO	LL-	LM-	UM-	UU-
10000011	01110010	10110111	000000xx	0	1	0	0
8 3	7 2	b 7	0 0				

PAL U32 forces the LL-, LM-, UM-, and UU- lines to the configuration state during mode line programming. The DTACK- line is driven through CR12 during the programming. This line is interpreted as the termination signal for a 16-bit port operation by LCA U25, which asserts DSACK1- to terminate the bus cycle.

The STERM line is buffered by U29D, which provides the required set-up and hold time for the synchronous termination signal. The STERM line also drives U29A, which is configured as an open collector driver for the DTACK line. This line is used by I/O bus masters and is extended to the end of the access cycle by LCA U25.

The Dynamic RAM controller has special output driver pins for the Dynamic RAM banks. Built-in slew limiting and series resistance allow for direct connection to the RAM chips.

RAM Parity 3-38.

LCA U23 contains the parity generation circuitry for each 8-bit byte of the 32-bit data bus (identical circuitry is used on each of the four bytes.) Read and write parity are generated by two different data paths inside the LCA, with the read parity pipelined by the Dynamic RAM CAS signal. Read data and the parity bit are latched on the rising edge of the CAS line for that 8-bit byte of RAM. Parity is generated for the eight data bits and compared to the latched parity bit coming from Dynamic RAM. If the access was a READ operation and the parity is different, an internal latch will be set on the next rising edge of CAS and latched active until the RD input is active. The Dynamic RAM bank that was active during the parity error is also latched. If any of the parity error lines are active, the parity interrupt line will be asserted if at least one access of the floppy control register has occurred since power up reset. The particular Dynamic RAM SIMM in error can be read by asserting the parity read line to the LCA (pin 72) and reading the byte and bank of the error on data lines D27-D31. Reading the register resets the errors.

Write parity is generated in a direct fashion from the eight data lines of each byte. It is presented to the parity bit data-in line of each 8-bit byte of Dynamic RAM during the write cycle.

ROM 3-39.

The Main PCA accepts one 32-pin ROM. Table 3-8 shows the acceptable configurations and the appropriate switch settings. The single-byte ROM is used only for boot up and is immediately copied into low RAM. The processor sees the ROM as an 8-bit port located on the top 8 bits of the 32-bit data bus. The ROM is located on the I/O bus side of the data bus to provide buffering. DSACK0- is generated inside LCA U25 for ROM accesses, resulting in a read bus cycle with 15 wait states.

Table 3-8. ROM Configuration

ROM TYPE	TOTAL BYTES	ADDRESS RANGE	SWITCH SEGMENTS 1234 5678
1 MEG ROM	128K	000000-01FFFF	0101 XXXX
2 MEG ROM	256K	000000-03FFFF	0110 XXXX
4 MEG ROM	512K	000000-07FFFF	1010 XXXX
			1 = ON (closed) 0 = OFF (open)

POD Interface 3-40.

The Pod Interface uses address locations 9C000 and 9C001 to accommodate information transfer, handshaking, and status.

Most of the pod interface circuitry is in LCA U25. Control signals to and from pod connector J7 are buffered by gates with hysteresis. The pod data bus is buffered by U27 and U28. Input buffer U28 is bipolar for greater survivability to electrostatic discharge (ESD). Pod UUT power is monitored with window comparator U34. L5 and C76 prevent Main PCA power glitches when a pod is removed or inserted. Refer to Table 3-9 for Pod control bit assignments.

Bit assignments for status and data bytes are shown in Tables 3-10 and 3-11, respectively. Latched outputs are cleared low by a reset.

Table 3-9. Pod Control Port Bit Assignment

NAME	I/O	DESCRIPTION
MAINSTAT	O	Handshake line from 9100FT/9105FT to the Pod.
POD_OE	O	Enables the Pod data buffer for write data. A high true signal enables (drives) the latched output data onto the Pod data lines (POD0 through POD7).
POD_RESET	O	Signal from 9100FT/9105FT to reset the Pod.
ABORT	O	Signal from the 9100FT/9105FT telling the Pod to abort a long operation.
PODSTAT-	I	Active low handshake line from Pod.
PODPRESENT-	I	A low true signal that indicates when a Pod is connected to the Pod Interface connector. This signal is derived from the Pod interface POWERFAIL signal. This signal can be enabled to generate an interrupt through the DTIO on change of state, (i.e., connecting or disconnecting the Pod).
DCE	I	Monitors the I/O Module Data Compare Equal (DCE) Signal.
PODINT	I	Buffered active high interrupt line from certain pods.
POWERFAIL	I	Active when Pod detects a bad UUT power supply.

Table 3-10. Status Byte (Address 9C000)

BIT	INPUT (U58)	LATCHED OUTPUT (U53)
D15	MAINSTAT	MAINSTAT
D14	POD_OE	POD_OE
D13	PODSTAT-	POD_RESET
D12	ABORT	ABORT
D11	PODPRESENT-	
D10	DCE	
D09	PODINT	
D08	POWERFAIL	

Table 3-11. Data Byte (Address 9C001)

BIT	INPUT (U42)	LATCHED OUTPUT (U37)
D07-D00	READ DATA	WRITE DATA

Table 3-12. Pod Interface Pinout

NAME	FUNCTION	PIN
POD0	Data bit 0	8
POD1	Data bit 1	20
POD2	Data bit 2	7
POD3	Data bit 3	19
POD4	Data bit 4	6
POD5	Data bit 5	18
POD6	Data bit 6	5
POD7	Data bit 7	17
MAINSTAT	Handshake	12
PODSTAT-	Handshake	24
PODRESET	Resets Pod	23
POWERFAIL	Power out of tolerance	11
PODINT-	Pod interrupt	1
ABORT-	abort	9
PODSYNC-	Pod Sync	10
SYNC SH	Pod sync shield	22
+5V	+5 volt power	2,15
+12V	+12 volt power	14
-5V	-5 volt power	21
GND	Ground Pod	4,13,16,25
X SHLD	cable shield	3

Data or response from the Pod is read at handshake completion. Data from the 9100FT/9105FT to the Pod is latched when written by the processor. POD_OE must be active to enable the output buffer.

Refer to Table 3-12 for the pinout and function of each signal line for the Pod Interface.

Presence of a pod is indicated on the PODPRESENT- line when a valid signal is detected on the POWERFAIL line (J9-11).

DUART-Timer-I/O 3-41.

The 9100FT/9105FT uses two 2681 DTIOs (U12 as DTIO1 and U7 as DTIO2). Each provides multiple Dual Asynchronous Receiver/Transmitters (DUART), timers, and input/output functions (two serial ports, one parallel input port, one parallel output port, and a timer.)

For DTIO1, register addressing and descriptions are given in Table 3-13. Specific DTIO1 functions are:

Table 3-13. DTIO #1 (Channels A, B)

REGISTER	ADDRESS	DESCRIPTION
MSA	$90001	mode register channel A (R/W)
SRA	$90003	status register channel A (R)
CSRA	$90003	clock select register A (W)
CRA	$90005	command register A (W)
ADATA	$90007	data holding registers A (R/W)
IPCR	$90009	input port change register (R)
ACR	$90009	aux control register (W)
ISR	$9000B	interrupt status register (R)
IMR	$9000B	interrupt mask register (W)
CTU	$9000D	counter/timer upper data (R)
CTL	$9000F	counter/timer lower data (R)
CTUR	$9000D	counter/timer upper register (W)
CTLR	$9000F	counter/timer lower register (W)
MRB	$90011	mode register channel B (R/W)
SRB	$90013	status register channel B (R)
CSRB	$90013	clock select register B (W)
CRB	$90015	command register B (W)
BDATA	$90017	data holding registers B (R/W)
INP	$9001B	input port (R)
OPCR	$9001B	output port configuration register (W)
SCC	$9001D	start counter command (R)
SOPB	$9001D	set output port bits command (W)
STC	$9001F	stop counter command (R)
ROPB	$9001F	reset output port bits command (W)

- Programmable Timer Interrupt
  OP3: timer output (50 ms)
  INT-: Interrupt Request to microprocessor
- EEPROM Control
  IP4: data output from EEPROM
  OP4: data input to EEPROM
  OP5: serial clock to EEPROM
  OP6: chip enable to EEPROM
- Pod Present Detection
  IP2: PODPRESENT change-of-state detection (can generate interrupt)
- Frequency Gate Generation/Detection
  IP3: FGATE frequency gate input
  OP2: frequency gate load
- DTIO1, Serial Port A: Application Keypad/Display
  TxDA: Data to Application Keypad/Display

RxDA: Data from Application Keypad/Display

CTSA- (IP0): Clear to Send from Application Keypad/Display.

Transmit and receive are at 19.2K baud. This port automatically holds off transmission data when the Keypad/Display is too busy to accept data.

- DTIO1, Serial Port B: Earth Referenced RS-232 Port #2

  TxDB: Transmit Data

  RxDB: Receive Data

  CTSB- (IP1): Clear to Send

  RTSB- (OP1): Request to Send

  Supports programmable baud rates, data width, stop bits, parity, and interrupts on buffer conditions, with three-deep FIFO on both transmit and receive.

For DTIO2, register addressing and descriptions are provided in Table 3-14. Specific DTIO2 functions are:

- DTIO2, Serial Port A: Programmers Keyboard

  RxDA: Programmers Keyboard Data

Table 3-14. DTIO #2 (Channels C, D)

REGISTER	ADDRESS	DESCRIPTION
MRC	$90000	mode register channel C (R/W)
SRC	$90002	status register channel C (R)
CSRC	$90002	clock select register C (W)
CRC	$90004	command register C (W)
CDATA	$90006	data holding registers C (R/W)
IPCR	$90008	input port change register (R)
ACR	$90008	aux control register (W)
ISR	$9000A	interrupt status register (R)
IMR	$9000A	interrupt mask register (W)
CTU	$9000C	counter/timer upper data (R)
CTL	$9000E	counter/timer lower data (R)
CTUR	$9000C	counter/timer upper register (W)
CTLR	$9000E	counter/timer lower register (W)
MRD	$90010	mode register channel D (R/W)
SRD	$90012	status register channel D (R)
CSRD	$90012	clock select register D (W)
CRD	$90014	command register D (W)
DDATA	$90016	data holding registers D (R/W)
INP	$9001A	input port (R)
OPCR	$9001A	output port configuration register (W)
SCC	$9001C	start counter command (R)
SOPB	$9001C	set output port bits command (W)
STC	$9001E	stop counter command (R)
ROPB	$9001E	reset output port bits command (W)

The baud rate is 1200 baud. The keyboard has a separate reset line, which is connected to OP7 of DTIO #2.

- DTIO2, Serial Port B: System Referenced RS-232 Port #1

  TxDB: Transmit Data

  RxDB: Receive Data

  CTSB- (IP1): Clear to Send

  RTSB- (OP1): Request to Send

  Supports programmable baud rates, data width, stop bits, parity, and interrupts on buffer conditions, with three-deep FIFO on both transmit and receive.

- Second Programmable Timer Interrupt

  OP3: Timer output, Divide by 16

  INT-: Interrupt Request to microprocessor

- Floppy Disk Change Detection

  IP2: Drive 1 Disk Change (can generate interrupt)

  IP3: Drive 2 Disk Change (can generate interrupt)

- Floppy Disk Interrupt Monitor

  IP4: Read Floppy Drive Data Interrupt Bit

  IP5: Read Floppy Drive Interrupt Bit

- Programmers Keyboard Reset

  OP7: KBRST- Keyboard Reset

- I/O Module Power Supply Control

  OP6: I/O Module Low Current

- Other

  OP2: RUN UUT LED Drive

  OP4: Disk Access LED Drive

  OP5: Force the fan to run at high speed.

Processor Clocks 3-42.

The clocks for the processor and Dynamic RAM controller are generated from a 50-MHz crystal oscillator that is divided down to 25 MHz by flip-flop U39 and series terminated by resistors R84, R85, R86, and R88 to prevent ringing. A nearly perfect 50% duty cycle for the processor clock maximizes timing tolerances at the Dynamic RAM controller.

I/O Bus Data Buffering 3-43.

U41 and U42 are 16-bit bidirectional transceivers with built-in data latches. For I/O accesses originating at the 68030 microprocessor, the parts function as 32-to-16 bit transparent bus drivers. The particular buffer selected is determined from the state of the SIZE/A0/A1 lines coming out of the microprocessor, decoded by PAL U32, and gated by LCA U25. When an external bus master has control of the I/O bus through either of the 96-pin I/O slots, data read from the RAM is latched inside one of the two data buffers on the rising edge of STERM and held for the duration of the bus cycle. Data written to RAM from the I/O bus is stable during the (relatively) short Dynamic RAM

memory cycle and is consequently not latched. Data read from RAM would normally start to float at the conclusion of the synchronous data cycle, long before being latched by the DMA controller.

During microprocessor accesses of the I/O bus, A1-A9, FC0-FC2, and R/W- are buffered by transceivers U33 and U22. Strobe signals UDS-, LDS-, and NDS- (generated by LCA U25) are also buffered by these transceivers.

During a bus grant cycle, the byte enable lines normally generated from the SIZE/A0/A1 lines by PAL U32 are derived from the I/O bus lines (ILDS-, IUDS-, and IA1) and driven from LCA U25.

Floppy Disk 3-44.

The floppy disk interface consists of the floppy disk controller chip (U17), the digital data separator (U16), and the buffers to the floppy drive (U15 and U13.) The signals that control data rates and drive selection are generated inside LCA U23. A simple seven-bit latch enabled with the floppy control line (pin 29) controls the density, clock rate, drive select, and drive reset functions of the floppy subsystem. (Refer to Table 3-16 for control output information.) Data to the latch is transferred over data lines D24-D30. Accessing the floppy control register for the first time after power up also enables the parity interrupt,

9132 Sync Access 3-45.

Main PCA test is facilitated by a 9132-type sync connector at J1; no 68030 sync adapter attachment to the system is required. A reset overdrive point is provided at J2, asserted with a high level. The highest 8 bits of data, a non-buffered system clock, and the necessary control lines are provided.

EEPROM 3-46.

A 16 word by 16-bit serial EEPROM stores system configuration data. The serial data and clock lines are controlled by the I/O lines of DTIO1 (U12).

DC/DC Converter 3-47.

The 70V supply for the front panel display is generated by an inverter driven by two non-overlapping clock signals generated inside LCA U23. Open collector drivers U10A and U10B supply a +12V dc gate signal to driver FETs Q1 and Q2 at a frequency of about 33 kHz. Step up transformer T1 generates the 70V for the front panel display, ±12V dc and +5V dc for the earth-referenced RS232 Port 2, and -12V dc for the system referenced Port 1 RS232 output driver.

Fan Control 3-48.

Transistor Q3 shorts out the temperature sensing thermistor during the selftest memory test to provide maximum startup torque to the fan. After selftest is completed, the fan is allowed to slow to the speed set by the thermistor positioned in the air flow.

LCA Initialization 3-49.

The two LCAs are loaded from the serial configuration stored in ROM U36 only during power-up reset. Once LCA U23 has stabilized and raised its INIT line, LCA U25 supplies the serial clock for both LCAs, reads in the configuration data needed, and passes the remaining configuration data on to LCA U23. The LCAs are unaffected by further resets.

MICROFLOPPY DISK SYSTEM 3-50.

Disk Drive 3-51.

The 9100FT uses one 3.5-inch, double-sided, high-density microfloppy disk drive. On the 9105FT, two of these drives are used. Each disk uses 80 tracks per side (0 to 4F hex), formatted as either 16 or 32 sectors of 256 bytes per track, for a formatted capacity of 640K or 1.2M bytes. Each drive is accessed and formatted through the Floppy Controller.

Floppy Drive Controller 3-52.

An FDC1797 floppy controller (U17) and an FDC92C39 Floppy Disk Interface Circuit (FDIC) are used for floppy drive control. The floppy controller does not format the floppy disk; this function is performed through software. The controller does perform the following functions:

- It searches for the correct track and sector.
- It calculates CRC values and inserts all required CRCs during a write.
- It serializes data on a write and decodes data on a read.

The FDIC circuit (U16) performs digital data separation and track-selectable write pre-compensation.

Table 3-15. Floppy Controller (U43) Addressing

NAME	ADDRESS	DESCRIPTION
DCOMND	$80001	Disk Command Register (write)
DSTAT	$80001	Disk Status Register (read)
DTRACK	$80003	Disk Track Register (read/write)
DSECTOR	$80005	Disk Sector Register (read/write)
DDATA	$80007	Disk Data Register (read/write)

Table 3-16. Floppy Drive Control Latch Outputs

<table>
<tr><th>NAME</th><th colspan="3">DESCRIPTION</th></tr>
<tr><td>DS0, DS1</td><td colspan="3">Drive Selects (turn on motor and enable communications with floppy controller for one drive at a time.)</td></tr>
<tr><td>SPARE</td><td colspan="3">(not used)</td></tr>
<tr><td>MINI</td><td colspan="3">Controls Floppy Controller clock to select data rate for mini (5 1/4- or 3 1/2-inch, logic low) or standard (8-inch, logic high) drive.</td></tr>
<tr><td>DENS</td><td colspan="3">Selects between single density (logic low) and double density (logic high).</td></tr>
<tr><td rowspan="6">P0, P1</td><td colspan="3">Selects the write pre-compensation time, as shown below.</td></tr>
<tr><td>P1</td><td>P0</td><td>TIME</td></tr>
<tr><td>0</td><td>0</td><td>0 ns</td></tr>
<tr><td>0</td><td>1</td><td>125 ns</td></tr>
<tr><td>1</td><td>0</td><td>250 ns</td></tr>
<tr><td>1</td><td>1</td><td>375 ns</td></tr>
</table>

Addresses for U17 Floppy Controller registers are shown in Table 3-15.

Latched outputs from LCA U23 (address 80000) control drive selects and other features. Table 3-16 describes these outputs.

Interrupts 3-53.

The Floppy Data Interrupt is generated by the floppy controller when it needs the next byte of data while doing a write or when the next byte of data is available in read mode. The Floppy Data Interrupt is automatically cleared when the byte is received or read.

The Floppy Controller Interrupt is generated by the floppy controller in response to a variety of conditions. The chip's interrupt status register must first be read to determine the cause. This interrupt can be polled at DTIO #2 Input Port, bit 5.

HARD DISK SYSTEM 3-54.

On the 9100FT, an SCSI hard disk occupies the space otherwise used in the 9105FT for a second floppy disk drive. System software that is resident on this 40M byte, 3.5-inch hard disk is backed up with floppy disks.

The hard disk connects directly to the SCSI bus on the Multi-Function Interface (MFI) II PCA, which is plugged into J6 on the Main PCA.

POWER SUPPLY 3-55.

An OEM switching power supply is used to operate from a line voltage of 90 to 132V ac (47-440 Hz) or 180 to 264V ac (47-63 Hz). Single outputs of +5.1V dc and -5V dc and two outputs of +12V dc are provided. The 9100FT power supply is rated at 150W (maximum). Pin designations for the power supply are presented in Table 3-17.

OPERATOR'S DISPLAY 3-56.

Vacuum-Fluorescent Display (VFD) 3-57.

The vacuum-fluorescent display uses a 254-by-26 pixel layout. Each character comprises a six wide by eight high group of pixels, allowing for a total width of 42 characters per line (numbered 0 through 41). A pseudo-character at position 42 allows for a backspace to affect character 41. The cursor cannot be positioned prior to character 0 or after character 42. The display contains up to four lines (numbered 0 through 3).

A total height of 26 pixels allows for display of either three lines separated with a blank row (character mode), or three full lines and a partial fourth line (graphics mode). The character mode is the default at startup.

The vacuum-fluorescent display is in essence a tube, with the filaments forming a heated cathode. A switcher circuit supplies 12V to one side of the filament and about

Table 3-17. Power Supply Pinout

DC OUT		AC IN	
TB1-1	+12V 4.0 Amps +-5%	TB2-1	AC Hot
TB1-2	+12V 2.0 Amps +-10%	TB2-2	AC Neutral
TB1-3	-5V 1.0 Amp +-5%	TB2-3	AC Earth ground
TB1-4,5,6	Power supply common		
TB1-7,8	+5.1V 15.0 Amps +-4%		

4V to the other side. These voltages are switched at the end of each scan cycle (after all grids have been scanned). The switching is synchronized to the scan rate to prevent flicker.

Each switching cycle is controlled by U14 and its associated output drivers. Two discrete actions occur at the start of each cycle. The filament drive is first switched off briefly. Next, the filament is driven (through Q2/Q6 or Q3/Q5) in the direction opposite to that used in the last cycle. Transistors Q2 and Q6 are used during one cycle direction, and Q3 and Q5 are used during the other cycle direction. U31 supports the filament drive switch off function.

The vacuum-fluorescent tube grids are driven in pairs. Grid input (GI) is held high for two clock periods at the beginning of the refresh cycle. The grid drivers are shift registers that are clocked to the next set of grids with each refresh scan. The grids are driven in pairs, G1 and G2, followed by G2 and G3, and so on. This scheme is illustrated in Figure 3-4.

Anodes comprise rows A1 through D24, which are also driven in pairs. Rows A and B (or C and D) are enabled together. If dots associated with only one row are on, both rows in the pair are still enabled.

The Z8 display processor, U1, both receives inputs, data, and commands from the main microprocessor and sends data out through a TTL-level serial interface. Divider U4 uses the Y1 reference clock signal (fed through U1) to derive timing signals for the circuit. U1 uses multiplexed address timing for data output; U2 latches the address for use with RAM and shift registers.

U1 receives the code for the character to be displayed, converts the code to the appropriate pixel pattern, and then writes the converted code to the appropriate row and column of the display RAM. However, U1's main function is to refresh the display tube. U1 uses pointers to the grid counters, reads data from display RAM, and, by holding A11 high, simultaneously writes data to serial shift registers U23 and U24. The state machines U14B and U15B shift the data out of the U23/U24 parallel-serial converters into the correct row drivers. This process is repeated four times for each refresh, with the data then being latched into the row drivers.

The SET- pulse from U1 provides the master timing signal for this refresh process. When SET- is true, grid input (GI) is also true. U13 and U14 provide the 1/4-3/4 duty cycle signal A, which is the master timing signal. One A cycle corresponds to one grid pair refresh. STROBE is used to strobe data into the row drivers. GCLK (the inverse of STROBE) is used to clock the grid drivers to the next position (G1/G2 to G2/G3, etc.). Row driver enable is provided by EAB- (for rows A and B) and by EAD- (for rows C and D). Outputs to display grid and row drivers incorporate pull-up resistors to provide valid MOS voltage levels. All grid and row drivers are disabled at reset or power-up by DSPYE (display enable) from U25.

Both grid and row currents flow through the filaments. Therefore, after a reset, the processor, U1, clears all grids and rows before a new enable is output. This action prevents filament destruction due to excess current.

Auxiliary circuitry includes the LED drivers. The RUN UUT and DISK ACCESS LEDs are driven by the Main PCA; all other LEDs are controlled by U1 (with latch U30) on the Display Interface PCA.

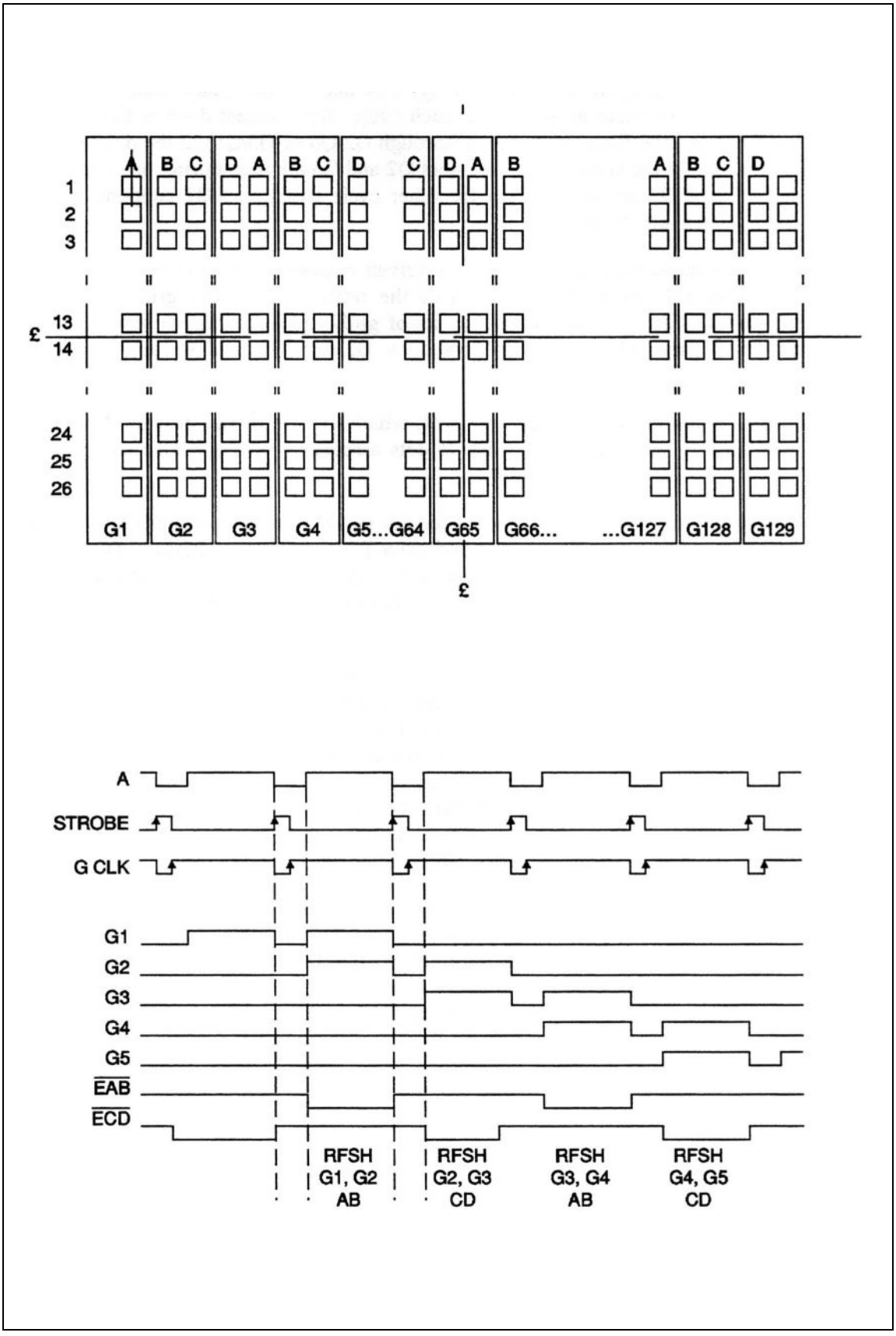


Figure 3-4. Vacuum Fluorescent Display

At the end of each display refresh, the processor scans the keypad by writing to U26, a 4-to-1 decoder. U26 drives one of the column lines low. The processor then reads the ROWBUSS to determine if any row line has been pulled low, signifying a keypress. Only one key press at a time is recognized by the processor. That key press must be withdrawn before another can be recognized. Multiple key presses are not recognized.

U28 is a shift counter whose output is used for character or graphics mode. In the character mode, nine bits are shifted out (the ninth bit designates a blank between text lines). This cycle is repeated three times, and five bits are shifted out on the fourth cycle to yield the 32 bits. In the graphics mode, an eight-bit load/shift-out cycle is repeated four times to derive 32 bits.

U29 provides a free-running oscillator for the beeper. The processor can enable either or both of two tones.

Resets are handled by U18 and U31, which reset the processor and clear both all U25 outputs and all latched LEDs (through U30.)

A 20-wire ribbon cable connects the Operator Display and Keypad to a Main PCA serial port. Data is exchanged at 19.2K baud. Ribbon cable connections are described in Table 3-18.

Displayable Characters 3-58.

The characters shown in Table 3-19 (hex values 20 through FF) are displayable. Some of the display characters are not available through TL/1 programs, but can be accessed by the Main PCA processor using the hex values listed. The character codes shown in Table 3-20 are control codes of the display. These codes, which do not represent displayable characters, perform certain control functions.

Two control modes are available. The first, display mode, specifies display of the two bit maps (page 1 or page 2) as follows:

Table 3-18. Operator's Display Ribbon Cable Connections

LINE	USE	TYPE	DESCRIPTION
10,12,14,20	Ground		
16,18	12 Volts	Power	Power for filament and for bell
6,8	5 Volts	Power	Power for logic
4	70 Volts	Power	Power for vacuum-fluorescent display
1,5	Earth		Green Ground
19	Key		Key for alignment
17	RESET	Input	Active high resets the processor
15	TRANSMIT	Output	Transmits data to Main PCA at 19.2K baud
13	RECEIVE	Input	Receives data from Main PCA at 19.2K baud
11	CTS-	Output	Active low holds off Main PCA transmit
9	ROW7	Input	Last row of the keypad scan
7	COLUMN9	Output	Last column of the keypad scan
3	RUN-LED	Input	Controls “RUN UUT” LED
2	DISK-LED	Input	Controls “DISK ACCESS” LED

Table 3-19. Operator's Display Characters

20 = ' '	30 = '0'	40 = '@'	50 = 'P'	60= "‘'	70 = 'p'
21 = '!'	31 = '1'	41 = 'A'	51 = 'Q'	61 = 'a'	71 = 'q'
22 = '"'	32 = '2'	42 = 'B'	52 = 'R'	62 = 'b'	72 = 'r'
23 = '#'	33 = '3'	43 = 'C'	53 = 'S'	63 = 'c'	73 = 's'
24 = '$'	34 = '4'	44 = 'D'	54 = 'T'	64 = 'd'	74 = 't'
25 = '%'	35 = '5'	45 = 'E'	55 = 'U'	65 = 'e'	75 = 'u'
26 = '&'	36 = '6'	46 = 'F'	56 = V'	66 = 'f'	76 = 'v'
27 = "'	37 = '7'	47 = 'G'	57 = 'W'	67 = 'g'	77 = 'w'
28 = '('	38 = '8'	48 = 'H'	58 = 'X'	68 = 'h'	78 = 'x'
29 = ')'	39 = '9'	49 = 'I'	59 = 'Y'	69 = 'i'	79 = 'y'
2A ='*'	3A = ':'	4A = 'J'	5A = 'Z'	6A = 'j'	7A = 'z'
2B = '+'	3B = ';'	4B = 'K'	5B = '['	6B = 'k'	7B ='{'
2C=','	3C = '<'	4C = 'L'	5C= '\'	6C = 'l'	7C ='|'
2D = '-'	3D = '='	4D = 'M'	5D = ']'	6D = 'm'	7D ='}'
2E='.'	3E = '>'	4E = 'N'	5E = ' '	6E = 'n'	7E = '~'
2F ='/'	3F = '?'	4F = 'O'	5F = '_'	6F = 'o'	7F = Block

80 = reduced '0' (upper left)	88 = reduced '8' (upper left)
81 = reduced '1' (upper left)	89 = reduced '9' (upper left)
82 = reduced '2' (upper left)	8A = bracket (lower right)
83 = reduced '3' (upper left)	8B = bi-directional pin
84 = reduced '4' (upper left)	8C = large pin above chip
85 = reduced '5' (upper left)	8D = I.C. pin above chip
86 = reduced '6' (upper left)	8E = up arrow
87 = reduced '7' (upper left)	8F = down arrow
90 = reduced '0' (lower right)	98 = reduced '8' (lower right)
91 = reduced '1' (lower right)	99 = reduced '9' (lower right)
92 = reduced '2' (lower right)	9A = bracket (upper left)
93 = reduced '3' (lower right)	9B = omega
94 = reduced '4' (lower right)	9C = large pin below chip
95 = reduced '5' (lower right)	9D = I.C. pin below chip
96 = reduced '6' (lower right)	9E = left arrow
97 = reduced '7' (lower right)	9F = right arrow

- Display Mode 0: Alternately displays Page 1 and Page 2 at a fixed rate of approximately 1 Hz. Display mode 0 is the default at startup.
- Display Mode 1: Displays Page 1 only
- Display Mode 2: Displays Page 2 only

The second, write mode, controls placement of the character as follows:

- Write Mode 0: Places the character in both Page 1 and Page 2. Write mode 0 is the default.
- Write Mode 1: Places the character in Page 1 only.
- Write Mode 2: Places the character in Page 2 only.

Table 3-19. Operator's Display Characters (cont)

A0 = reduced '0' (center)	A8 = reduced '8' (center)
A1 = reduced '1' (center)	A9 = reduced '9' (center)
A2 = reduced '2' (center)	AA = divide sign
A3 = reduced '3' (center)	AB = ±
A4 = reduced '4' (center)	AC = micro
A5 = reduced '5' (center)	AD = 'inverted '-'
A6 = reduced '6' (center)	AE = pi
A7 = reduced '7' (center)	AF = pound sign
B0 = reduced inverted '0' (center)	B8 = reduced inverted '8' (center)
B1 = reduced inverted '1' (center)	B9 = reduced inverted '9' (center)
B2 = reduced inverted '2' (center)	BA = I.C. head
B3 = reduced inverted '3' (center)	BB = I.C. body segment (full splat)
B4 = reduced inverted '4' (center)	BC = reduced splat (center)
B5 = reduced inverted '5' (center)	BD = box
B6 = reduced inverted '6' (center)	BE = double box
B7 = reduced inverted '7' (center)	BF = super-reduced splat
C0 = boxed super-reduced splat	C8 = reduced inverted 'H'
C1 = reduced inverted 'A'	C9 = reduced inverted 'I'
C2 = reduced inverted 'B'	CA = reduced inverted 'J'
C3 = reduced inverted 'C'	CB = reduced inverted 'K'
C4 = reduced inverted 'D'	CC = reduced inverted 'L'
C5 = reduced inverted 'E'	CD = reduced inverted 'M'
C6 = reduced inverted 'F'	CE = reduced inverted 'N'
C7 = reduced inverted 'G'	CF = reduced inverted '0'
D0 = reduced inverted 'P'	D8 = reduced inverted 'X'
D1 = reduced inverted 'Q'	D9 = reduced inverted Y'
D2 = reduced inverted 'R'	DA = reduced inverted 'Z'
D3 = reduced inverted 'S'	DB = logic 1 level
D4 = reduced inverted 'T'	DC = logic x level
D5 = reduced inverted 'U'	DD = logic 0 level
D6 = reduced inverted 'V'	DE = 0 -> 1 edge
D7 = reduced inverted 'W'	DF = 0 -> x edge
E0 = x ->edge	E8 = reduced inverted *
El = 1 ->edge	E9 = reduced inverted up arrow
E2 = 1 ->edge	EA = reduced inverted down arrow
E3 = x ->edge	EB = not yet defined
E4 = left inverse line	EC = not yet defined
E5 = left line	= not yet defined
E6 = right inverse line	EE = not yet defined
E7 = right line	= not yet defined
F0 through FF = not yet defined	

Table 3-20. Control Characters

HEX	FUNCTION	DESCRIPTION
00	Load bell	Load bell value
01	Time out	Set time out value
02	no op	(not used)
03	Blink	Blank location in page 2, advance cursor, and set write mode 0.
04	Flash	Put the complement of the character at the page 1 cursor into page 2, advance cursor, and set write mode 0.
05	Character mode	Place extra blank dot between lines
06	Graphics mode	No extra blank dot between lines
07	Bell	Ring bell
08	Cursor left	Move cursor one character left
09	Cursor right	Move cursor one character right
0A	Cursor down	Move cursor one line down
0B	Cursor up	Move cursor one line up
0C	Clear	Place in display mode 0, place in write mode 0, clear entire display, and home cursor
0D	<cr>	Carriage return
0E	Test	Perform tests on hardware
0F	Move cursor	Move cursor to a new location
10	<bs>	Backspace and delete
11	Annunciators	Turn annunciators on or off
12	Blink mask	Make annunciators solid or blink
13	XOR next char	XOR with display the next character and advance cursor
14	Clear to eol	Clear to end of line
15	Clear line	Clear entire line and place cursor at zero character
16	Invert next char	Invert the video of the character and advance cursor
17	Underline	Underline character at the cursor and advance cursor
18	Display mode 0	Set display mode 0
19	Display mode 1	Set display mode 1
1A	Display mode 2	Set display mode 2
1B	Graphics	Next 6 bytes define the graphics to be placed in the display
1C	XOR graphics	Next 6 bytes define the graphics to be XORed with the old display value
1D	Write mode 0	Set write mode 0
1E	Write mode 1	Set write mode 1
1F	Write mode 2	Set write mode 2

Annunciators 3-59.

Seven LED annunciators are used with the display: BUSY, STOPPED, RUN UUT, STORING SEQ, DISK ACCESS, MORE SOFTKEYS, MORE INFORMATION. The RUN UUT and DISK ACCESS LEDs are controlled by the Main PCA; the other LEDs are controlled by the Display PCA.

OPERATOR'S KEYPAD 3-60.

The 55-key keypad consists of 50 hard-labeled keys and five soft-labeled keys. An LED annunciator, located on the keypad, lights when the alpha mode is activated. Functionally, the keypad is a 9-column by 8-row matrix. Pressing a key completes a connection between a particular column output and row input.

The keypad is scanned by the Display PCA after every display refresh. If a new key closure is detected at this time, the appropriate byte is sent via the serial output to the Main PCA. Values returned for each key are shown in Table 3-21.

A tenth column output (COLUMN9) is not used on the keypad. COLUMN9 is routed (along with the ROW7 input signal) across the Main PCA to the Probe I/O-ECL PCA. This arrangement allows for scanning the external footswitch input. A closure of the footswitch connection is detected and the appropriate byte sent to the Main PCA in the same fashion as with a key closure on the keypad.

Table 3-21. Operator's Keyboard Key Values

KEY	VALUE	ASCII	KEY	VALUE	ASCII
SOFTKEYS	58	X	B (1011)	42	B
F1	59	Y	SETUP MENU (P)	24	$
F2	5A	Z	SEQ (Q)	25	%
F3	5B	[	POD (R)	2C	,
F4	5C	\	ROM (S)	2D	-
F5	5D	]	STIM (T)	34	4
RESET	5E	^	4 (0100)	35	5
ALPHA	20	space	5 (0101)	3C	<
EXEC (G)	21	!	6 (0110)	3D	=
PROBE (H)	28	(	7 (0111)	44	D
BUS (I)	29	)	(up arrow)	4C	L
READ (J)	30	0	REPEAT (-)	54	T
C (1100)	31	1	STOP	55	U
D (1101)	38	8	OPTION (U)	26	&
E (1110)	39	9	(V)	27	’
F (1111)	40	@	SYNC (W)	2E	.
ENTER YES	41	A	(X)	2F	/
CLEAR NO	48	H	RUN UUT (Y)	36	6
EDIT (.)	50	P	0 (0000)	37	7
HELP	51	Q	1 (0001)	3E	>
MAIN MENU (K)	22	"	2 (0010)	3F	?
GFI (L)	23	#	3 (0011)	46	F
IO MOD (M)	2A	*	<-	47	G
RAM (N)	2B	+	(down arrow)	4E	N
WRITE (0)	32	2	->	4F	O
8 (1000)	33	3	LOOP (Z)	56	V
9 (1001)	3A	:	CONT (SPACE)	57	W
A (1010)	3B	;	footswitch	6F	o

PROBE I/O-ECL PCA 3-61.

Overview 3-62.

The Probe I/O-ECL PCA provides the interface from the mainframe to the single-point Probe, Clock Module, and the I/O Connector PCA. This pca is mounted flush to the Main PCA inside the mainframe. The Probe I/O-ECL PCA block diagram, Figure 3-5, contains the following functional block groups:

- Address Decoding
- Probe Interface
- Clock Module Interface
- Custom Probe Delay
- Custom Probe Logic
- Stop Counter I/O Module Interface
- Miscellaneous Functional Blocks

Probe I/O-ECL Addressing 3-63.

The 9100FT/9105FT allocates two 64K blocks of address space for the Probe and I/O Module system. The address space for the Probe is selected by PS4-, and the address space for the I/O Module is selected by PSS-. Within the probe address space (PS4-), PAL U42 acts as an address decoder, generating four upper (UPBn) and four lower (LPBn) probe chip select signals. Signal PS4PRB- is used to select all of the circuitry on the Probe I/O-ECL PCA. Signal PS4VPRB- is used to select the 9100FT-031 Vector Probe Option (if installed). Note that the Vector Probe Option is a daughter pca that is installed on top of the Probe I/O-ECL PCA. The address map for the Probe I/O-ECL PCA is shown in Table 3-22.

Probe Interface 3-64.

The Probe Interface group block in Figure 3-5 contains smaller specific blocks that contain circuitry for the following:

- Controlling data input by the Probe.
- Generating voltages used by the Probe.
- Controlling and driving the Probe lights.
- Detecting blown probe fuse.
- Counting frequency, transitions, or periods with bit counters.

PROBE DATA INPUT 3-65.

The signal from the Probe tip passes through a resistor divider network on the single-point Probe PCA and the Probe I/O-ECL PCA. An FET (Q1) buffers the signal before high-speed dual comparator U30 samples the signal. The comparator thresholds are set by programmable digital-to-analog converters (DACs) U20 and U23. The low DAC (U20) generates the low threshold by receiving input data on D00 through D07 from the buffered data bus; the high DAC (U23) generates the high threshold from D08 through D15 of the same bus. The outputs of U30 are converted from ECL (Emitter-Couple Logic) levels to TTL levels before entering the Custom Gate Array Delay Chip (U18).

The DACs (U20 and U23) provide an output voltage (0 to 2.55V dc) based on the value of the hex byte written to their control inputs. This output must be converted to a bipolar voltage (+0.52 to -0.45V dc) for proper circuit operation. A -1.2V voltage reference (CR13, C45, and R58) is used with a voltage divider (R50, R51, and R56 for the U23 High DAC, or R57, R59, and R60 for the U20 Low DAC.) The outputs from these two resistor divider networks are used as thresholds for the U30 dual comparator.

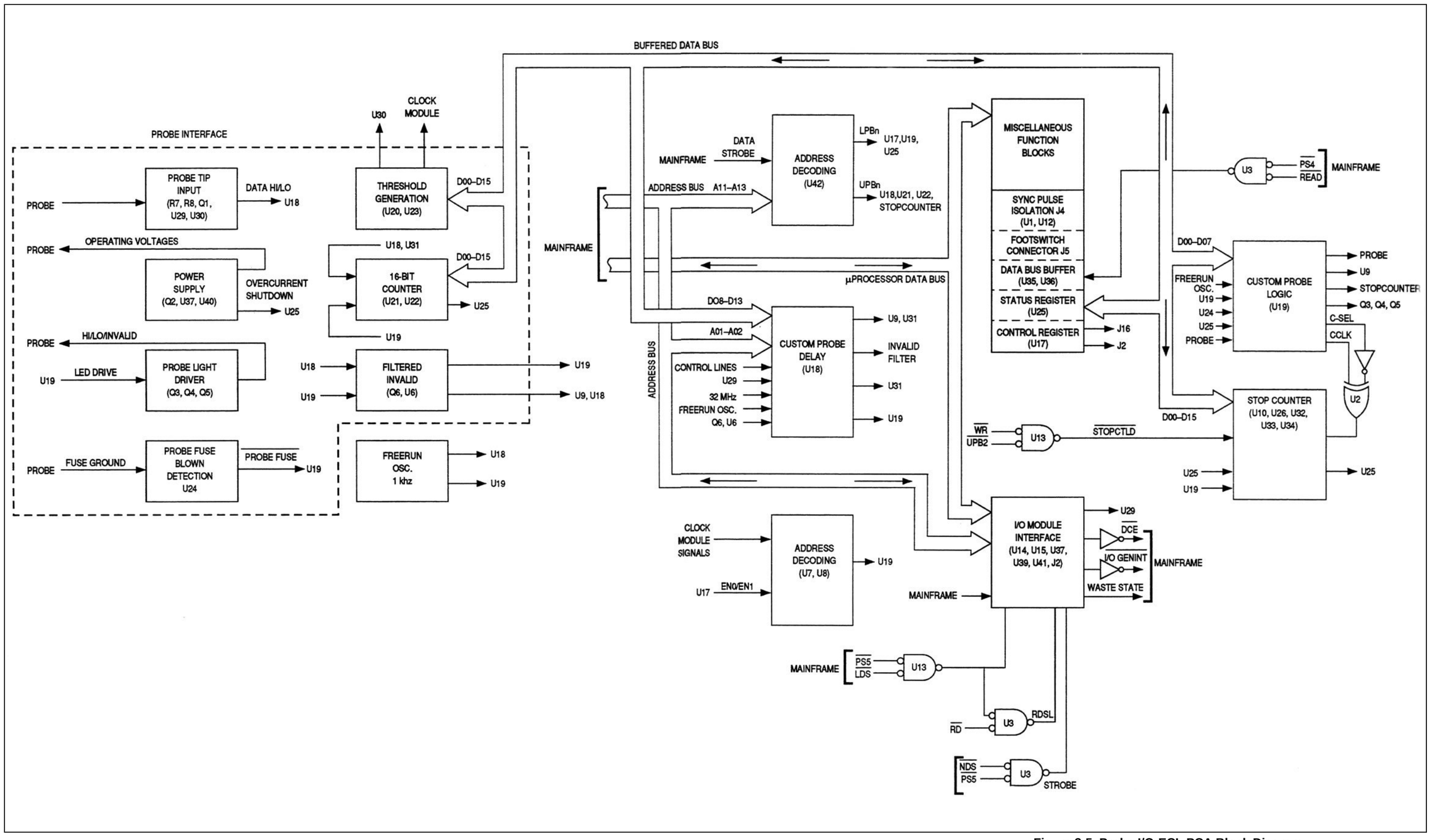


Figure 3-5. Probe I/O-ECL PCA Block Diagram

Table 3-22. Probe I/OI/O Module Interface Address Map

ADDRESS	WIDTH	COMPONENT	R/W-
C000x-	(even bytes) (0 through 6)	Probe Delay Chip	(Read/Write)
C000x	(odd bytes) (1 through F)	Probe Logic Chip	(Read/Write)
C0800	(byte)	High Threshold D/A	(Write)
C0801	(byte)	Low Threshold D/A	(Write)
C1000	(word)	External Stop Counter	(Write)
C1001	(byte)	Status Register	(Read)
C1800	(word)	16-bit External Counter	(Read)
C1800	(byte)	Clear External Counter and Delay Chip Latched Registers	(Write)
C1801	(byte)	Control Register	(Write)
C04XX	(byte)	9100FT-031 Vector Probe Option	(Read/Write)

If the Probe I/O-ECL PCA is repaired or replaced, probe offset calibration is required. This calibration routine compensates for small offsets in the dual FET (Q1) and for tolerances in the resistor divider and negative voltage reference. As a result, four values are stored in EEPROM on the Main PCA.

Four probe input threshold types (TTL, CMOS, RS232, and ECL) are available to the user. For each threshold type, Table 3-23 shows the real threshold voltage, the nominal

Table 3-23. Voltage Threshold Levels

HEX VALUE REAL THRESHOLD DAC OUTPUT U30 INPUT TO DAC LOGIC LEVEL VOLTAGE VOLTAGE VOLTAGE (nominal)				
TTL				
HIGH Threshold	2.4 volts	1.98 volts	0.31 volts	C6
LOW Threshold	0.8 volts	1.45 volts	0.10 volts	91
CMOS				
HIGH Threshold	3.5 volts	2.35 volts	0.45 volts	EB
LOW Threshold	1.0 volts	1.52 volts	0.13 volts	98
RS232				
HIGH Threshold	3.0 volts	2.21 volts	0.39 volts	DD
LOW Threshold	-3.0 volts	0.17 volts	-0.39 volts	11
ECL				
HIGH Threshold	-1.25 volts	0.76 volts	-0.16 volts	4C
LOW Threshold	-1.45 volts	0.69 volts	-0.18 volts	45

DAC output voltage, the input voltage seen at the comparator, and the nominal hex byte written to the DAC.

PROBE OPERATION VOLTAGES 3-66.

Two voltage levels (regulated +5 volts and -1.2 volts) are produced on the Probe I/O-ECL PCA. The +5 volts is used for the Pulse High probe signal and as power for U1 on the Probe PCA. The +12VN (nonregulated) voltage is converted to +5 volts by a +5 volt regulator (U40). Voltage comparator U37 acts as an over-current shutdown sensor for the +5 volt supply. A -1.2 volt power supply (Q2) converts -5 volts to -1.2 volts used to produce Pulse Low for the Probe.

FUSE BLOWN DETECTION 3-67.

Fuse blown detection circuitry for the Probe is located between the probe connector and the Probe Custom Chip. The probe ground fuse (F1), located on the Probe I/O-ECL PCA, protects circuitry in case the user incorrectly connects the ground clip to a power supply. Detection for blown fuses is generated by two LM339 voltage comparators (U24) that generate the output Fuse-P.

PROBE LIGHT DRIVE AND CONTROL 3-68.

The Probe Light Control block contains a 2:1 Line Multiplexer (U9), and a 4-bit Data Latch (U31). The 2:1 Line Multiplexer selects latched/unlatched data. Invalid asynchronous data is filtered by the Filtered Invalid block, which requires that the invalid signal persist for 100 ns (2 ms for RS-232 levels) before being detected. Synchronous data invalid levels are taken as is on the clock edge. The output of the Filter block is multiplexed with the invalid signal from U31 to become INVALID IN at U19-58 along with the High and Low outputs of U9. The HI IN, INV IN, and LO IN pulses are stretched 50 ms internally within U19 to to become the light drive inputs to Q3, Q4, and Q5.

The three transistors Q3, Q4, and Q5 drive the three logic level indicator lights on the Probe. Each transistor drives one light:

- Q3 for the (green) low logic level light.
- Q4 for the (yellow) invalid logic level light.
- Q5 for the (red) high logic level light.

The input signals to the transistors originate from U19-28, U19-29, and U19-30.

EXTERNAL 16-BIT COUNTER 3-69.

Two 8-bit binary counters (U21, U22) are cascaded together to form a 16-bit external counter. This 16-bit counter combines with the 8-bit internal counter of U19, yielding a 24-bit counter that counts transition changes, clock frequency counts, and period counts from data collected by the probe tip.

Clock Module Interface 3-70.

The Clock Module Interface on the Probe I/O-ECL PCA contains a Quad ECL-TTL Translator (U28), a Dual 4:1 Line Multiplexer (U16), and a fuse blown detection circuit. The START/START-, STOP/STOP-, ENABLE/ENABLE-, and EXT CLK/EXT CLK- signal lines are ECL (Emitter-Coupled Logic) level outputs of the Clock Module. These outputs are converted to TTL level signals before being introduced to U19. Before entering U19, the ENABLE/ENABLE- and SYNC signals are multiplexed by EN0 and EN1 to form an input line to U19-24 via U16 for the purpose of selecting an External Enable. A blown Clock Module fuse detection circuit signals to the mainframe that a

Clock Module fuse is blown. Two voltage comparators (U24) detect the blown fuse and generate the blown fuse signal (FUSE-C) to U19.

Custom Delay Chip 3-71.

The Custom Delay Chip (U18) is one of two Probe Control chips on the Probe I/O-ECL PCA. The functional block located on Figure 3-5 contains internal components dealing with Probe Input Signal Delay. The function of U18 is to produce high, low, and invalid data signals including CRC data and CRC clock generation. These signals are sent to support chips and to the Custom Probe Logic Chip (U19).

The Delay Chip contains a data multiplexer that can select either the Probe threshold or a presently unused current input U18-5. A FREERUN signal (a 1-kHz continuous square wave) and an input clock is used for internal calibration. The CURRENT input is for future expansion purposes. Once data is past the multiplexer, two separate data paths form the DATA HIGH, the DATA LOW, and INVALID OUT outputs. The enabled clock U18-19 has a 60-ns delay switchable in or out (0 delay or 60-ns delay). A history and CRC data latch contained in U18 provides valid data (high or low) or the last valid data input for the CRC register in U19.

Functions of U18 include:

- Delaying data high and low from the probe tip input for U31 and U9 to interpret.
- Latching synchronous/asynchronous Hi, Lo, and Invalid Probe Data.
- Generating CRC clock and CRC data signals used by U19 from Enable Clock input.
- Generating INVOUT signal output at U18-34.
- Qualifying CRC Clock Data, either present data or last valid data.

An Invalid signal, which amounts to a lack of valid high or valid low, is generated by the custom delay chip as the INVOUT signal. This is routed through a filter (U6 and associated resistor/diode arrays); the resulting output is termed Filtered Invalid. In asynchronous mode, the invalid pulse must exceed 100 ns in width. This is accomplished by using an RC network to delay the trip point of U6-1 by 100 ns. An invalid input exceeding 100 ns trips this circuit, producing the filtered invalid output. In asynchronous mode, this output is used by both the internal latches and the probe light circuitry. For the RS-232 threshold, Q6 is used to switch in C34, increasing the RC timing and producing a longer filter time of about 2000 ns for the invalid signal.

Synchronous invalid constitutes an absence of a valid low or valid high at the clock time.

For accurate probe operation, the delays in the probe system must be calibrated. Before delay calibration can be performed, the software must determine the amount of delay per tap on the delay line internal to the custom delay chip (U18). At power-up or reset, an external 32-MHz clock signal is routed through both the high and low data paths. By choosing differing amounts of delay and counting clock edges, the software is able to compute the amount of delay per internal delay line tap. This data is saved for use in delay calibration.

The clock delay (60 ns) is switched in for negative delays, and the data delay is switched in for positive delays. Calibration is accomplished by adding delays and reading the pca's history latches. Note that any change in the external lights during this process results from pulses being fed through related circuits and has no other significance.

The delay calibration value is computed by the probe calibration procedure. Both the Clock Module and the Probe are used during the procedure, with the Probe tip being pulsed to generate the calibrating clock signal. Delays are adjusted until both the clock (probe tip pulse) and the data arrive at the history latch at the same time. The delay value derived is saved in memory and can then be stored on disk for subsequent use.

Custom Logic Chip 3-72.

The second of two custom chips on the Probe I/O-ECL PCA, the Probe Custom Chip, is located on the functional block diagram Figure 3-5. Internal structure and the functions of U19 deal with Probe Data signals, Probe Light drive, counting events, and clock selection. The Custom Logic chip contains the following internal structures:

- Digital Pulse stretcher circuitry for Probe Lights.
- A counter configurable for frequency, period, or transition.
- Pulser control logic.
- A CRC register circuit.
- Start_stop_enable logic for the clock.
- A multiplexer to select the clock.

The Custom Logic Chip supports functions from both the Probe and the Clock Module with different clock-type selection (Pod SYNC, FREERUN, and EXT CLK) determined within U19. CRC data is also calculated by U19.

Predetermined synchronous or asynchronous data selected by the 2:1 Line Multiplexer (U9) on the Hi in, Invalid in, and Lo in signal lines are stretched by U19 to at least 50 ms. The stretched signals become the three light drives for Q3, Q4, Q5.

An 8-bit internal counter (U19) and a 16-bit external counter (U21, U22) perform three counting modes: transition, frequency, and period. These functions count either data high transitions or 8-MHz clock transitions and are controlled as described below:

- Transition Mode: The counter counts data transitions with a software controlled start/stop.
- Frequency Mode: The counter counts the data transitions for a 50-ms period. The software converts this count to frequency by multiplying the count by 20.
- Period Mode: The counter counts the 8-MHz clock from one data high transition to another. The software uses this mode to measure low frequencies, converting the count from period to frequency for display.

CRC data is gathered at the internal CRC register (part of U19). The CRC uses the delayed data and clock signals from U18.

PULSE HI and LO signals for the Probe are generated by U19 to stimulate signal lines in the UUT. To produce pulser signals, a logic low from an internal clock logic register plus a Hi, Lo, or software- generated clock enter a pulse logic register. The two outputs of the pulse logic register are the PHI and PLO signals on U19, pins 10 and 26, respectively.

The Probe Logic Chip contains an internal selection system to provide the enabled clock for U18 and the 16-bit Stop Counter, and to provide a SYNC Pulse to an externally-connected oscilloscope via a BNC connector located on the mainframe back panel. EXT START and EXT STOP from the Clock Module, and STOPCNT- are combined to

enable the internal clock signal input to the internal Clock Logic Register of U19. The selected enable, SYNC-, FREERUN, and EXT CLOCK from the Clock Module combine to enable the internal Clock Logic Register, which generates the enabled clock outputs CCLK and CCLK-.

When the probe pulser is active, the internal clock logic requires the opposite edge of the pulse to start the clock. In a non-pulsing condition, the clock starts on the first selected edge. To provide an edge (before the clock edge) to start the probe output pulse, the clock is inverted internally in U19 when the pulser is active. The CSEL output is high when the clock has been inverted internally, forcing pins 3 and 6 of U2 to invert the clock outputs again to provide the correct signals to U18 and the sync output.

Stop Counter 3-73.

The Stop Counter is a series of four presettable 4-bit binary up/down counters (U26, U32, U33, U34). Each counter has four parallel data inputs to count the total 16 data bus lines. STOPCTCK (Stop Count Clock) from U2-6 is the clock pulse for the counter chips. The STOPCTLD- (Stop Count Load) input to U26, U32, U33, and U34 (generated from U13-11) overrides counting and loads the data present on the parallel data lines into the counter; the processor loads the 2s complement of the stop count into the counter. Each counter chip has a maximum count output that is gated by U38. When all of the counters reach maximum count, the output from U38 puts an active low on the data input of a dual D-type flip-flop (U10). U10 then provides the STOPCNT- input for U19-20 on the next clock pulse. RDMISC- (Read Miscellaneous) from U11-8 enables the U25-10 output, which is bit 1 of the Status Register, to read the status of the Stop Counter. The Stop Counter is programmable for 1 to 64K counts and is used to control SYNC history latches and CRC registers.

I/O Module Interface Connector 3-74.

The I/O Module Interface Block located on the Probe I/O-ECL PCA, shown in Figure 3-5 of the functional block diagram, contains three parts.

- The connector and related components for the I/O Connector PCA connector.
- The -VDRV Regulator for the I/O Module Pattern Drive.
- The Over-Current Detection Circuitry for the I/O Module Pattern Drive.

The I/O Connector PCA Connector interfaces data lines D00 through D15, address lines A01 through A12, and control lines between the I/O Module and the mainframe.

The 16 data lines from the I/O Connector PCA to the Probe I/O-ECL PCA connect to the uP Data Bus with the low eight data bits direction controlled by an Octal Bus Transceiver (U39). The transceiver's data flow direction is controlled by PS5- and WRITE-. The upper eight data bits are unused. The address lines and four control lines (R/W- (Read/Write), FGATE (Frequency Gate), ODRESET (Over Drive Reset), and SEL- (Select)) are buffered by line drivers to maintain signal levels for communication with the I/O Modules and the I/O Connector PCA. The STROBE signal is generated for the I/O Modules by gating NDS- (New Data Strobe) with PS5- (Peripheral Select 5). The STROBE signal is sent to the I/O Connector PCA for further processing before reaching the I/O Module. Outputs from the I/O Module include the two interrupts DCE and IOGEN. The sense + and sense -- signals are sourced from the +VDRV voltage regulator on the I/O Connector PCA.

I/O MODULE -VDRV VOLTAGE REGULATOR 3-75.

This regulator provides a -0.85V dc output with a high short term current sinking ability (greater than 2A) and a long term current sinking capability of 250 mA. Overload

detection is also provided. Figure 3-6 presents a simplified schematic of the -VDRV Voltage Regulator.

The regulator uses an inverting op amp circuit. With a gain of -0.17, the op amp provides -0.85V dc output from the 5V dc input. The PNP power transistor (im- plemented as PNP/NPN compound Q9/Q10) is configured as an emitter follower and is used to provide increased current sinking capability. The collector supply is a 250 mA constant current sink. Dual Diode CR10 is used to return feedback to U41 and to clamp U41's output during low current situations.

When the current demand is low (less than 250 mA), the current sink saturates, and the -FAULT signal is at about -4.5V dc. If a high current transient appears, the current sink (Q11 and part of op amp U41) turns on, and 250 mA flows into the -5V dc supply. The rest of the current flows into the 10,000 µF capacitor, slowly charging it up. Because this capacitor is in the collector circuit of the power transistor, the regulator's output remains unaffected while this voltage is rising. If the current demand is high enough or long enough, the capacitor charges to above -1.2V. At this level, the LM339 comparator trips, generating an IOOCI- interrupt and forcing the control line ODRESET- low. This in turn shuts off the I/O module overdrivers, limiting the current. The time constants of the circuit are set so that 2A can be sunk for 10 ms without affecting the regulated -VDRV output or generating an over-current fault.

PARALLEL I/O MODULE OVER-CURRENT DETECTION 3-76.

Parallel I/O Module over-current conditions are detected from either of two sources: the +VDRV supply or the -VDRV supply. The +VDRV regulator is situated on the I/O Connector PCA. Current sense from that supply is provided via the sense+ and sense- signals, which are differentially amplified by a section of U41 and compared by a section of comparator U37 to a reference. This reference is switchable, via the LO-CURRENT- line, to one of two settings. The low setting, commanded when

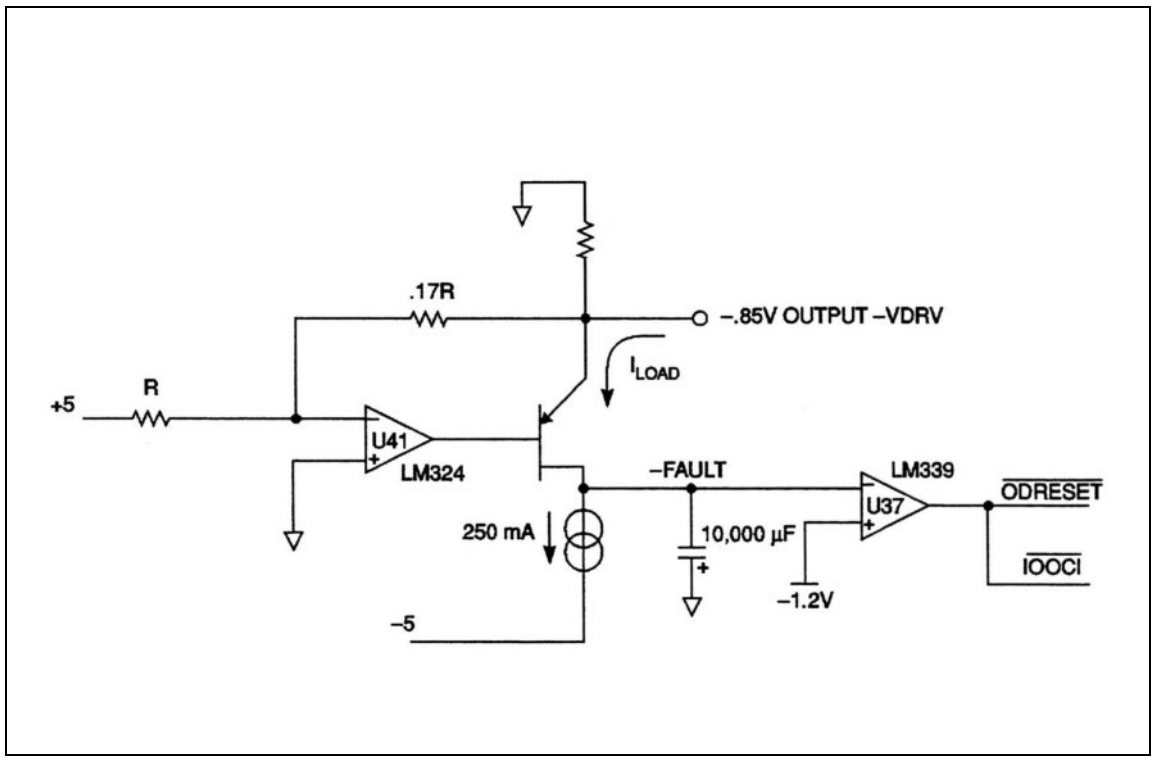


Figure 3-6. -VDRV Voltage Regulator Simplified Schematic

LO-CURRENT- is low, sets a reference of about .4V, which in turn sets an effective current limit of about 200 mA. The high setting sets the reference to about 4V, which sets the current limit to about 2A. This high current setting is guaranteed by software to never be active for more than 10 ms, (with a max duty cycle of 1%). R73, C18, and CR12 slow down the output of the differential amplifier so that it does not trip on transients.

A -VDRV over-current condition is detected by another section of the U37 comparator. These two comparators are “wire ORed” together. If either one detects a fault, both of their outputs goes low. This fault causes the ODRESET- line to go low, which turns off the I/O Module overdrivers, thus removing the over-current fault. At the same time, flip-flop U27 is clocked, making IOOCI- go active and generating an interrupt. This interrupt can be cleared by writing line IOCLRINT- low; (WRITE 0 C1801: bit 1 = 1 says clear interrupt; bit 1 = 0 says release interrupt).

Miscellaneous Functional Blocks 3-77.

The Probe I/O-ECL PCA has two functional blocks for the specific purpose of interfacing with external equipment: the SYNC Pulse Isolation block and the Footswitch Connector (J4). Two other functional blocks (Data Bus Buffers, Status Register, and Control Register) support operations for probe control.

SYNC PULSE ISOLATION 3-78.

SYNC Pulse Isolation uses an optoisolator and an earth-referenced divider to provide an earth-referenced TTL level SYNC Pulse (isolated from the 9100FT/9105FT) to an oscilloscope. Inputs to this block include an earth referenced +5 volts and a clock pulse from U2-6. The resulting external trigger output is available at a BNC connector on the rear panel.

TRIGGER OUT OPERATION 3-79.

The TRIGGER OUT source is defined with the SYNC PROBE key command or “sync” TL/1 statement. Command/statement options are:

free run	Sourced from 9100 mainframe 1-kHz internal oscillator.
pod	(Refer to specific pod manual for further information.)
ext	Sourced from 9100 Clock Module.
int	Sourced from 9100 software-controlled clock source. (Refer to TL/1 “strobeclock” statement.)

TRIGGER OUT has nominal TTL levels and is driven by a 74F totem pole output in series with a 330-ohm resistor. The signal is referenced to earth ground and optically isolated from the trigger source, producing an uncalibrated delay.

The TRIGGER OUT waveform is an active low pulse. The falling or leading edge indicates the start of the cycle. The rising (or trailing) edge indicates the end of the cycle and provides the timing reference.

FOOTSWITCH CONNECTOR 3-80.

The Footswitch Connector (J5) is a standard telephone jack that connects to a normally open switch. The switch is used as an external event recognizer. A test program can use such a switch to make a program depend on an external event, a manually generated signal, or a limit. Access to J5 is on the right side of the mainframe labeled (EXT SW). A switch closure is detected by the COLUMN9 and ROW7 signals; these signals are sourced from the keypad scanning circuitry on the Display PCA.

DATA BUS BUFFERS 3-81.

Data Bus Buffers (U35, U36) permit data transfer from the microprocessor data bus to a buffered data bus. Instructions from the microprocessor to the ICs on the Probe I/O-ECL PCA move along the microprocessor data bus through J6 to U35 and U36. The data moves through the Data Buffers onto the buffered data bus to the required ICs.

STATUS REGISTER 3-82.

The Status Register (U25) monitors single status bits on the Probe I/O-ECL PCA to detect I/O Over-Current Interrupts, Probe Power, Stop Counter Status, and Pulse-Transition Counter Carry-Bit Status. The Status Register is a quad 3-state buffer (U25) connected from the output of the circuit to the data bus. U25 is read only. Figure 3-7 summarizes the status bits. The Status Register output to the data bus is enabled by the RDMISC- (Read Miscellaneous) signal from U11, pin 8.

CONTROL REGISTER 3-83.

A 4-bit Write-Only Control Register (U17) generates the STOPCTENA- (Stop Counter Enable), IOCLRINT- (IO Clear Interrupt), EN0 (Enable 0), and EN1 (Enable 1). The Control Register decodes data bits 00 through 03 of the Buffered Data Bus to generate the output signals. Data bits 02 through 03 determine different ENABLE combinations. Data bit 01 either clears or allows an I/O Over-Current Interrupt, and data bit 00 enables or disables the Stop Counter. Figure 3-8 represents the data bit breakdown for the Control Register.

I/O CONNECTOR INTERFACE 3-84.

Overview 3-85.

The I/O Module Connector PCA provides the interface for the I/O Module to the 9100FT/9105FT. The I/O Connector Interface shown in Figures 3-1 and 3-2 is a

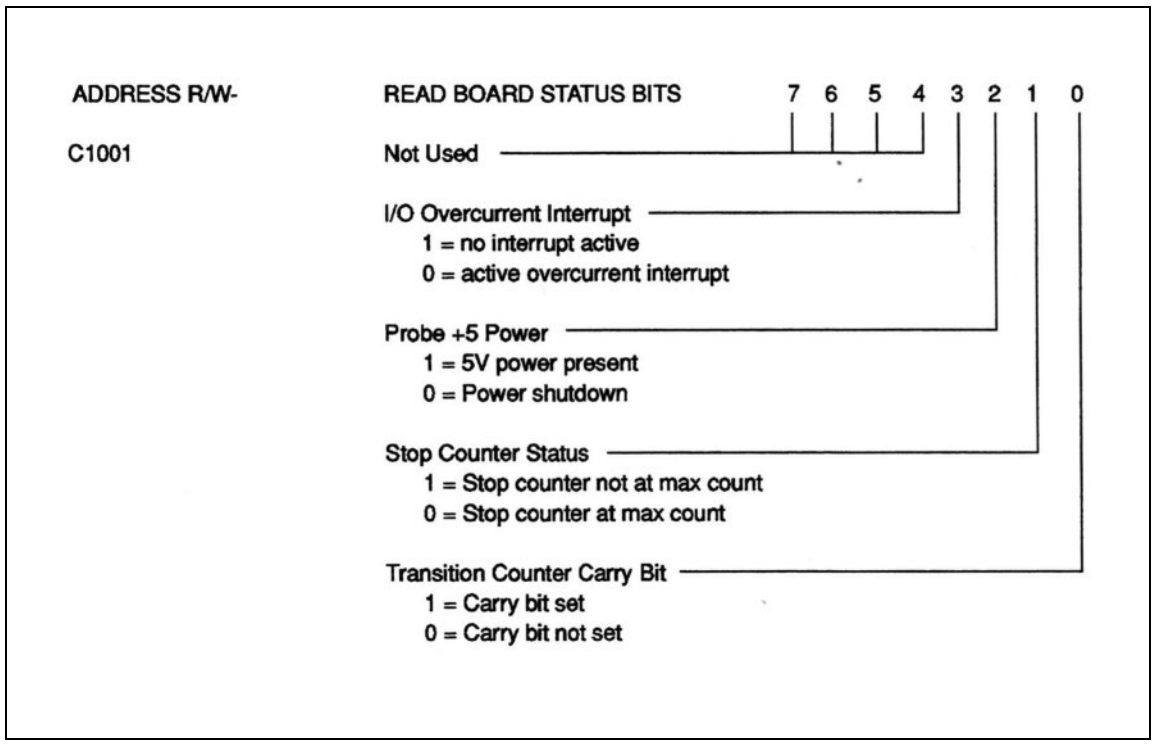


Figure 3-7. Status Register Bit Breakdown

vertically-mounted PCA that plugs into the Probe I/O-ECL PCA, which connects to the Main PCA. Up to four I/O Modules can be connected to the 9100FT/9105FT. The I/O Connector and the Probe I/O-ECL PCAs buffer the 68030 microprocessor address and data bus to send data out to the modules. The PCAs also contain the I/O Module overdriver power supplies and circuitry to gather and distribute control, data, and address signals, event detection, and operational power for each I/O Module.

Power Supplies 3-86.

There are two power supplies for the I/O Module, one at 5V dc, (called +VDRV), and one at -0.85V dc (called -VDRV.) The +VDRV power supply is a linear supply derived from the +12V dc supply. Current is sensed by measuring the voltage across the 0.47 ohm resistor. This voltage is measured on the Probe I/O-ECL PCA from the SENSE ± lines.

Gross over-current protection is provided by an LM338 voltage regulator (U4). Normal over-current protection is provided via an overdriver shutdown line, (ODRESET-). This line instantly turns off the overdrivers, removing the over-current fault. An over-current fault is triggered if current exceeds two programmable levels: 200 mA and 2A. The 200-mA level is the power-up default, and is only changed to the higher level during pattern drive. The 2A level provides a short term (10-ms, 1% duty cycle) maximum amount of current for all four I/O Modules. The over-current level is controlled by the (LO_CURRENT) control line produced by DTIO #2 (U7) on the Main PCA. If the 200 mA and 2A thresholds are violated, an I/O Over-Current Interrupt (IOOCI) is generated. Simultaneously, all of the overdrivers on all of the I/O Modules are shut off.

The 10,000 µF capacitor is part of the -VDRV regulator, which is covered in the Probe I/O-ECL PCA discussion.

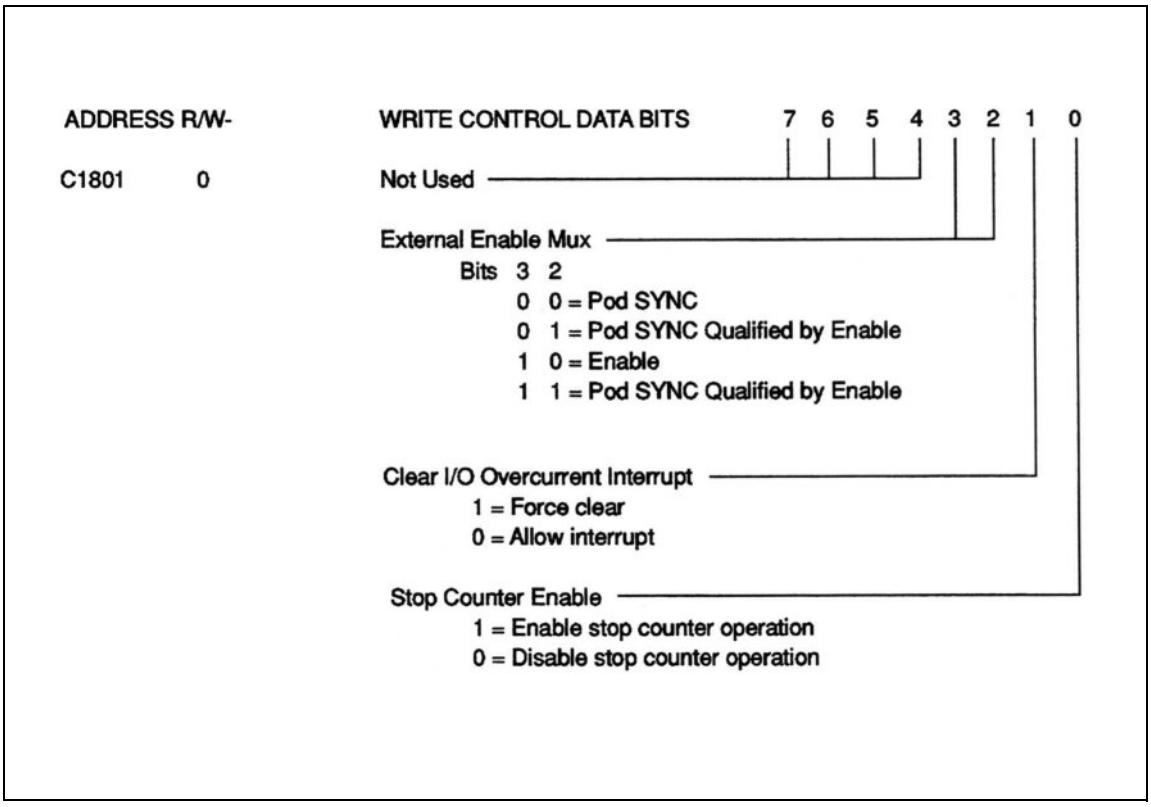


Figure 3-8. Control Register Bit Breakdown

I/O Module Connector PCA Contents 3-87.

The I/O Connector PCA contains four DB-37 vertically-mounted connectors that are accessible on the rear panel of the mainframe. On the other side of the PCA is a voltage regulator (U4) with supporting capacitors (.01 µF, 1000 µF), and the 10,000 µF capacitor used in the -VDRV regulator. The connector to the Probe I/O-ECL PCA (J1) supplies all I/O Module power, event detection, address, data, and control signals to the I/O Module.

The address bus containing A01 through A11 and the data bus containing D00 through D07 distribute address and data lines to each connector with A08 through A11 used to determine the ±STROBE for the selected I/O Module. When the STROBE signal is divided between each module connector, the signal has PS5 and "hot bits" decoded in the signal. The Pod ± SYNC signal used for timing with the Probe and I/O Module is also distributed to the four I/O connectors by a quad TTL-ECL translator (U2).

The DCE- and IOGEN- interrupts from each module are input to a dual 4-input NAND gate (U3). The outputs of U3 are connected to J1 and sent to the mainframe for further processing. The MODSEL- line is connected through jumper J8 to IWAIT3-. This forces I/O Module bus communications to occur with three wait states, allowing for reliable bus operation over long cable lengths.

PROBE/PULSER 3-88.

Overview 3-89.

The Single-Point Probe/Pulser is a 9100FT/9105FT interface device used to measure portions of the UUT PCA not accessible to the I/O Module. The Probe/Pulser measures inputs up to 40 MHz and generates stimulus pulses. A 1-bit-wide data channel provides input measurement and output stimulus capabilities. Features available through use of the Probe/Pulser include: 16-bit cyclic redundancy checks (CRC), clocked and asynchronous level history, and frequency measurements. The Probe/Pulser instrument is divided into four functional blocks:

- Sensing Block (Probe)
- Pulsing Block (Pulser)
- Level Indicator Block (Lights)
- Switch Block (Switch)

Refer to Figure 3-9 for the functional block diagram of the Probe/Pulser.

Probe 3-90.

The Probe measures signals from the UUT, with the Probe tip making a single-point connection on the UUT. The UUT signal is routed through Probe circuitry and the Probe cable to the 15-pin Probe connector on the right side of the mainframe. The Probe functional block contains both the common ground and the one-bit data channel for the UUT.

PROBE TIP INPUT 3-91.

Signals entering the Probe Tip pass through R1 and R2. These two resistors, in conjunction with R8 on the Probe I/O-ECL PCA, form a resistor-divider compensation network to match the impedance of the Probe cable. R9 is a pull-up resistor to pull the Probe to a tri-state condition when no other inputs are connected. The input signals exit the Probe via J1-14 and enter the Probe I/O-ECL PCA. The speed of the input signals must meet the criteria listed in Figure 3-10 to be captured by the Probe Data Channel.

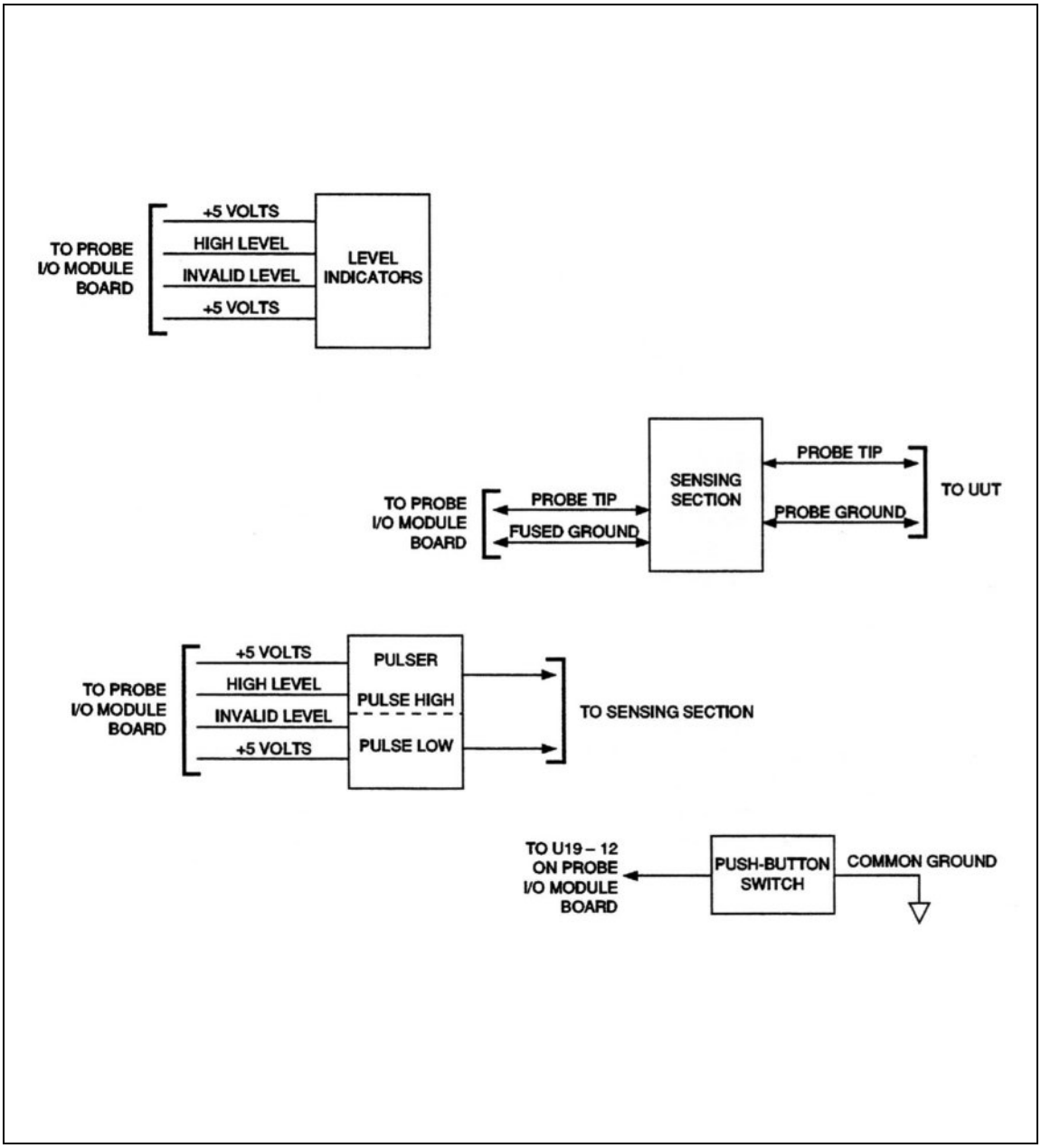


Figure 3-9. Probe/Pulser Functional Block Diagram

COMMON GROUND CLIP 3-92.

The Common Ground Clip connected to the Probe/Pulser clips to the UUT common ground. At the point where the ground connects to the Probe/Pulser, the common lead screws in to make connection. The ground line passes directly through the instrument to J1-9. If the user misconnects the Common Clip, a Probe Fuse located next to the Probe Connector on the mainframe provides protection from power supply shorts or other over-current conditions. The Ground Clip must be connected to the UUT to ensure a short return path for pulsing current.

Pulser 3-93.

The Pulser stimulates input signals for checking output data on the UUT. The Pulser drives a short duration high current level either high or low at a node being tested. The

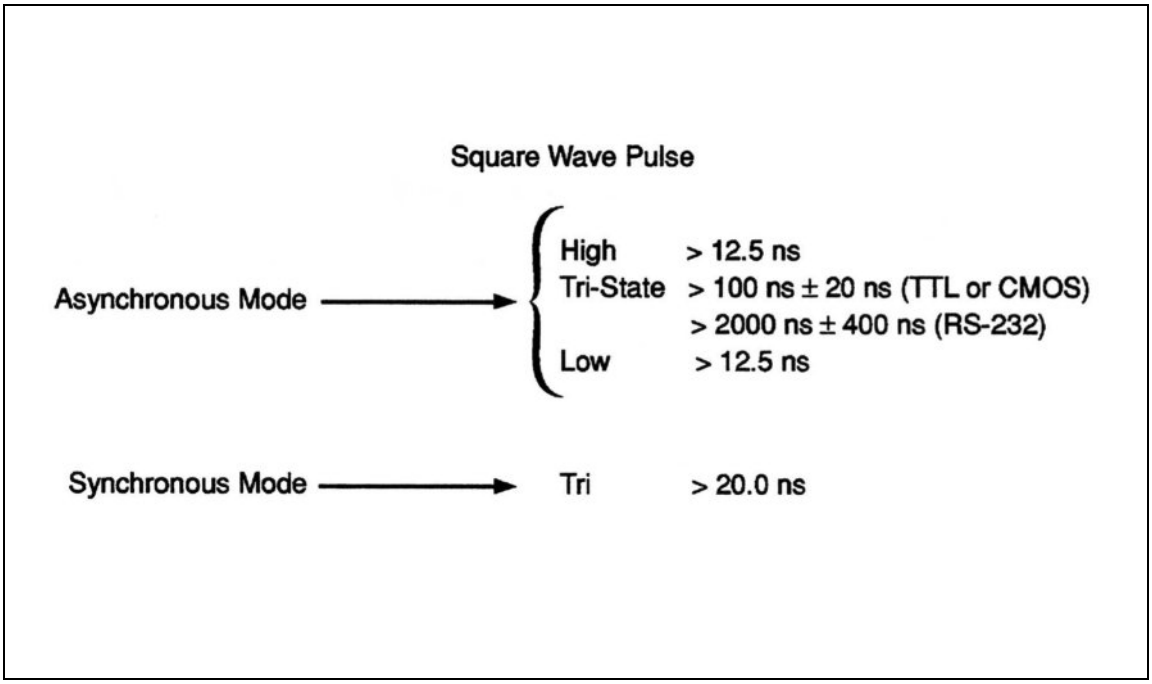


Figure 3-10. Probe Speed Specifications

output pulse can be toggled between High and Low or turned off completely (tristate). During the low pulse, current is supplied by Q4. A high logic level on the PULSE LO signal line turns on Q4, driving the Probe tip low through CR4. C4 supplies instantaneous current for the low pulse. When the Pulse low signal line is off (logic low), Q3 conducts to turn Q4 off quickly. CR4 prevents the Probe tip from being pulled high at this time. The -1.2V dc input from the Probe I/O Module (J1-13) is used to generate the low pulse.

On the PULSE HI signal line, the logic high into U1-5 inverts to a logic low to turn Q1 on, driving the probe tip high through CR1. C2 is a speed-up capacitor that drives Q1 into saturation, and C3 supplies instantaneous current for the high pulse. A logic low on the PULSE HI line turns Q1 off; Q2 is turned on, and CR1 prevents the Probe tip from being pulled low. The regulated +5-volt supply is used to generate the Pulse High signal and supplies power to U1. Both pulse levels drive the voltage at a specified current for the time shown in Table 3-24.

The Probe pulser exhibits a certain delay in reacting to the synchronous inputs. The maximum propagation timing from synchronous input to pulser action is listed in Figure 3-11.

The minimum pulse widths of the Pulser are shown in Table 3-25.

Table 3-24. Typical Probe Pulser Amplitude

LEVEL	VOLTAGE	CURRENT
High	> 3.5V > 4.0V	200 mA for less than 10 us (1% duty cycle) 5 mA continuously
Low	< .8V < .4V	200 mA for less than 10 us (1% duty cycle) 5 mA continuously

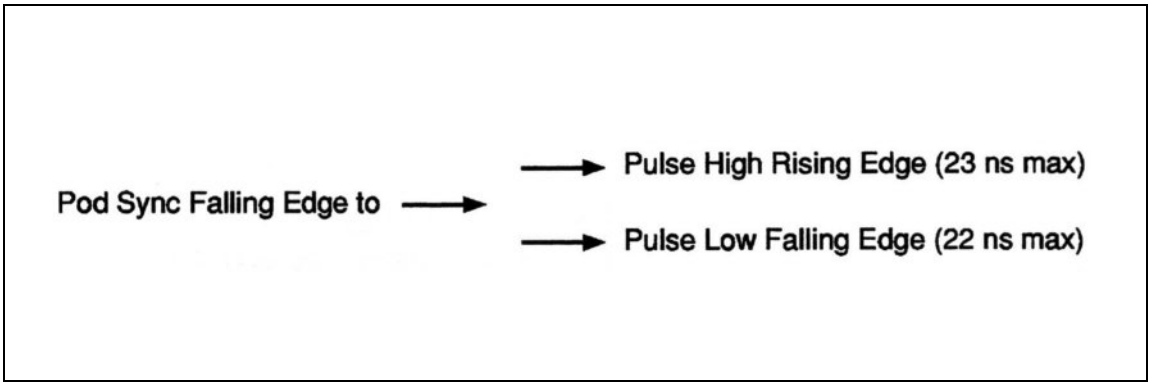


Figure 3-11. Probe Response Timing Specifications

Table 3-25. Pulser Pulse Width

MODE	WIDTH
Pod Sync	> 50 ns
Free Run	2 µs @ 1 kHz pulse rate
External	> 50 ns

Level Indicators 3-94.

There are three level indicators on the Probe. The level indicators are used to indicate what logic levels have been encountered. The indicators have the following meaning:

- Red: A valid high signal was encountered.
- Yellow: An invalid signal was encountered.
- Green: A valid low signal was encountered.

The logic indicators are driven by a circuit on the Probe I/O-ECL PCA that stretches the pulses to a minimum length of 50 milliseconds.

LOGIC LEVEL MODES 3-95.

The light logic can display in either synchronous or asynchronous logic mode. A writable register in the Probe Custom Logic Chip on the Probe I/O-ECL PCA chooses either synchronous or asynchronous mode. The choice is hardware independent of the SYNC Mode of the CRC and other clocked latches. Asynchronous information is displayed when SYNC is set to FREERUN, and all other SYNC modes display the last synchronous data.

LEVEL INDICATOR OPERATION 3-96.

The three LED level indicators are driven by three open-collector transistors (Q3, Q4, and Q5) on the Probe I/O-ECL PCA.

Push Button Switch 3-97.

A push button located on the Probe allows the user to indicate when the Probe is in place and ready to perform a “read probe”. When the user presses the push button, an interrupt is generated by the Probe I/O-ECL PCA. The interrupt is shared by the fuse-monitoring circuits and thus requires that a status register in the Probe Custom Logic chip be polled to determine the origin of the interrupt.

CLOCK MODULE 3-98.

Overview 3-99.

The Clock Module is an external unit that is plugged into the right side of the mainframe. When used in conjunction with the Probe, the Clock Module samples external events (start, stop, clock, and enable) that are necessary in gathering signatures from the UUT to synchronize data input and output through the Probe.

Clock Module Operation 3-100.

Four comparators (U1A, U1B, U2A, U2B) are used, with respective start, stop, clock, and enable input thresholds provided by the Probe I/O-ECL PCA. The inputs go through a divide-by-2 resistor-divider network to the comparators. The other input (0.8V) to the comparator is provided by the Probe I/O-ECL PCA, giving a threshold of 1.6 volts for external signals. The resulting balanced ECL signals are routed through J6 to the Probe I/O-ECL PCA. An external ground connection is also provided, with a user-accessible fuse (F1) protecting the circuit in case of inadvertent contact of the ground lead to the power source.

The balanced ECL signals from the Clock Module are converted to TTL level signals on the Probe I/O-ECL PCA before being introduced to the Custom Probe Logic chip (U19). A detection circuit is used to sense a blown fuse in the Clock Module. The outputs from the Clock Module are Start, Stop, Clock, and Enable. The Enable signal is multiplexed by the selection multiplexer (U16) signal lines; Pod SYNC, Enable ANDed with Pod SYNC, or inverted Enable ANDed with Pod SYNC produces the EXT ENABLE signal to U19-24.

Clock Module Speed 3-101.

The clock module timing specifications listed below are valid for all signal lines into the pod.

- Maximum Repetition Rate: 40 MHz square wave
- Minimum Pulse Width: 12.5 ns

MULTI-FUNCTION INTERFACE II 3-102.

Overview 3-103.

The Multi-Function Interface II (MFI II) assembly plugs into J11 on the FT Main PCA. On the 9100FT, the Hard Disk is connected through a cable to a connector on the Multi-Function Interface.

The Multi-Function Interface (MFI) II PCA supports peripheral systems for use with the 9100FT/9105FT. Standard features on this pca include a Small Computer System Interface (SCSI), a Real Time Clock, Direct Memory Access (DMA) Controller, and an IEEE-488 Interface.

Addresses 3-104.

The MFI II PCA plugs into J11 (the MFI II Card Connector) on the FT Main PCA. The pca is allocated the address space 0B0000 through 0BFFFF. Address decoding is performed by two PALs (U8 and U11) on the MFI II PCA.

Real Time Clock 3-105.

The Real Time Clock consists of a 1287 chip (U1) that contains a clock and a lithium battery. Test point TP1 facilitates monitoring of the clock.

A DTACK generator (U3 and U4) provides the extended read and write cycles required by the clock, The address and data to the clock chip are multiplexed by U9 and U10. The clock is addressed at odd bytes (B2001 -- B20FF).

SCSI 3-106.

The SCSI (Small Computer System Interface) is structured around a 53C80 controller chip (U6 on the MFI II PCA). Generally, U6 handles hardware and software interfacing between the 9100FT and the SCSI bus. On the 9100FT, the bus accommodates a hard disk and hard disk controller accessed through the internal SCSI connector (J2); the hard disk and SCSI circuits are not available with the 9105FT. The external SCSI connector (J3) provides SCSI bus connection for additional devices. Controller chip U6 is mapped to the 16 odd addresses B1001 through B101F.

DMA 3-107.

A 68440 Direct Memory Access controller chip (U12 on the MFI II PCA, A24) is used to provide DMA for data transfer during floppy disk operations. The address bus and data bus at the DMA chip are multiplexed by bi-directional buffer chips U13, U14, U15, and U16. The DMA controller chip is addressed starting at B4000.

IEEE-488 3-108.

The IEEE-488 interface uses a 9914 GPIB (IEEE-488) Controller chip (US on the MFI II PCA, A24). U2 and U7 buffer the signals to the connector, J4, for the external IEEE-488 cable and connector. The IEEE-488 controller is addressed at even bytes (B2000 - B2006).

VIDEO SYSTEM 3-109.

The separate Video Controller PCA supports the Monochrome Monitor or a color monitor. It is supplied with the 9100FT Programmer's Station. The Video Controller PCA is available with the 9105FT as an option. Note that the video system is character-mapped; in other words, a specific video RAM address maps into a physical location on the monitor screen.

Video Controller 3-110.

The 9100FT Video Controller PCA uses the 2674 Advanced Video Display Controller (AVDC), U1, along with the 2675 Color/Monochrome Attributes Controller (CMAC), U2. The 2674 (AVDC) generates the vertical and horizontal timing signals necessary for the display of data on a CRT monitor. The 2674 is programmed with terminal setup information, providing cursor, blanking, and clock signals to the CMAC. The AVDC is assigned address space OF0000 through 0FFFFF. In time with horizontal (HSYNC) and vertical (VSYNC) signals, the AVDC addresses Video RAM (U3 and U4) and the Character PROM (U5) on lines DADD00 through DADD11. By using the ASCII codes supplied by the microprocessor (and stored in Video RAM) and the correct display character data stored in the Character PROM, this sequencing yields display characters.

Video RAM 3-111.

U3 and U4 provide two kilobytes of static video RAM. When addressed over the main address bus (AA01 through AA10), Video RAM is used to store ASCII character codes supplied by the microprocessor over the main data bus (DB00 through DB15). Video RAM uses address space 0E0000 through 0EFFFF.

The Video Control sequentially samples these addresses using lines DADD00 through DADD11 and generates display characters using the ASCII codes found at these addresses and the corresponding display character information found in the Character PROM (U5).

Video RAM is shared by both the mainframe processor and the video-generating circuitry. The ASCII codes for display characters are stored in memory at the same addresses used by the Monitor. This memory mapping allows for efficient updating of data on the CRT. Figure 3-12 demonstrates display address mapping.

The video RAM, which resides in a 4K-byte memory space, supplies 2K words for storing characters (1920 words are needed by the 24 lines by 80 characters per line). Both the microprocessor on the Main PCA and the AVDC on the Video Controller have access to video memory; the Main PCA is allowed only to write to video memory. Video control circuitry synchronizes Video and Main PCA requests for memory.

Each displayed character resides in one word of memory, divided into two bytes. Use of the high (or attribute) byte differs between color operation and monochrome operation. The low (or character) byte does not differ between operating modes. Figure 3-13 illustrates the overall data format.

The eight registers controlling the video display are selected by the processor using address lines A1, A2, and A3. In addition, line A4 can be high or low for register selection in color mode, but must be high for register selection in monochrome mode.

Video Output 3-112.

Video Output comprises the 2675 Color/Monochrome Attributes Controller (CMAC) and associated circuitry. The 2675 contains a programmable dot clock divider to generate a character clock, a high speed shift register to serialize input dot data into a video stream, latches and logic to apply visual attributes to the resulting display, and logic to display a cursor on the display. Associated circuitry includes latches U11 and U13, which clock in display information provided by the character PROM.

Outputs to the Monitor include horizontal and vertical sync signals (positive polarity, TTL levels) for both monochrome and color operation. Video data is output as positive white analog levels in monochrome operation or as RGB TTL levels in color operation.

The isolated output allows the mainframe to remain isolated from the earth-grounded monitor. All color and synchronization signals pass through high-speed optoisolators (U28 - U31). For monochrome output, red and blue output channels are combined to

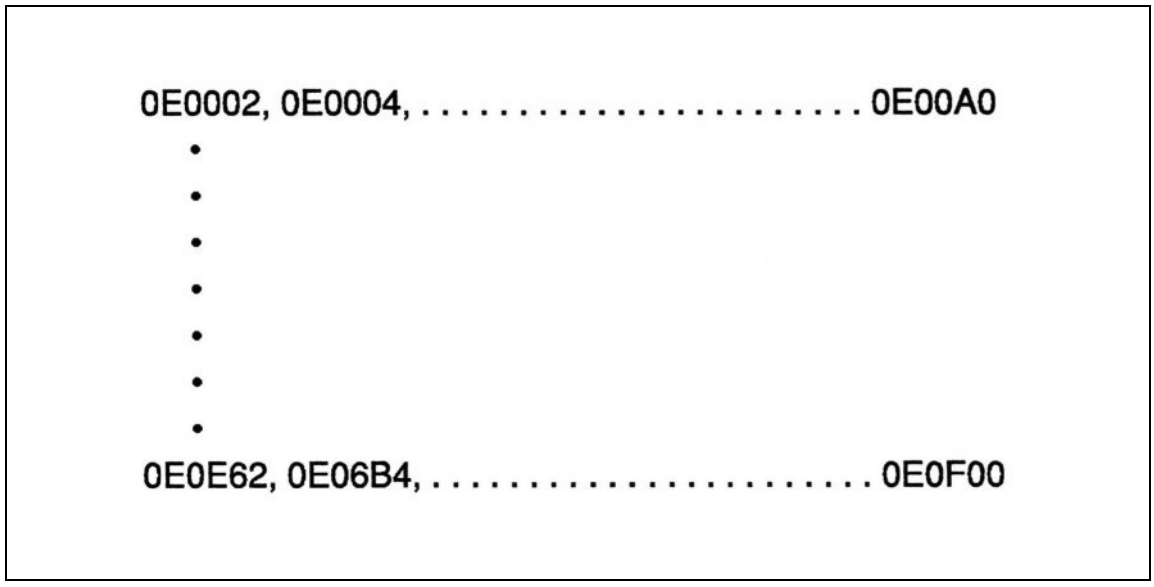


Figure 3-12. Video Display Address Mapping

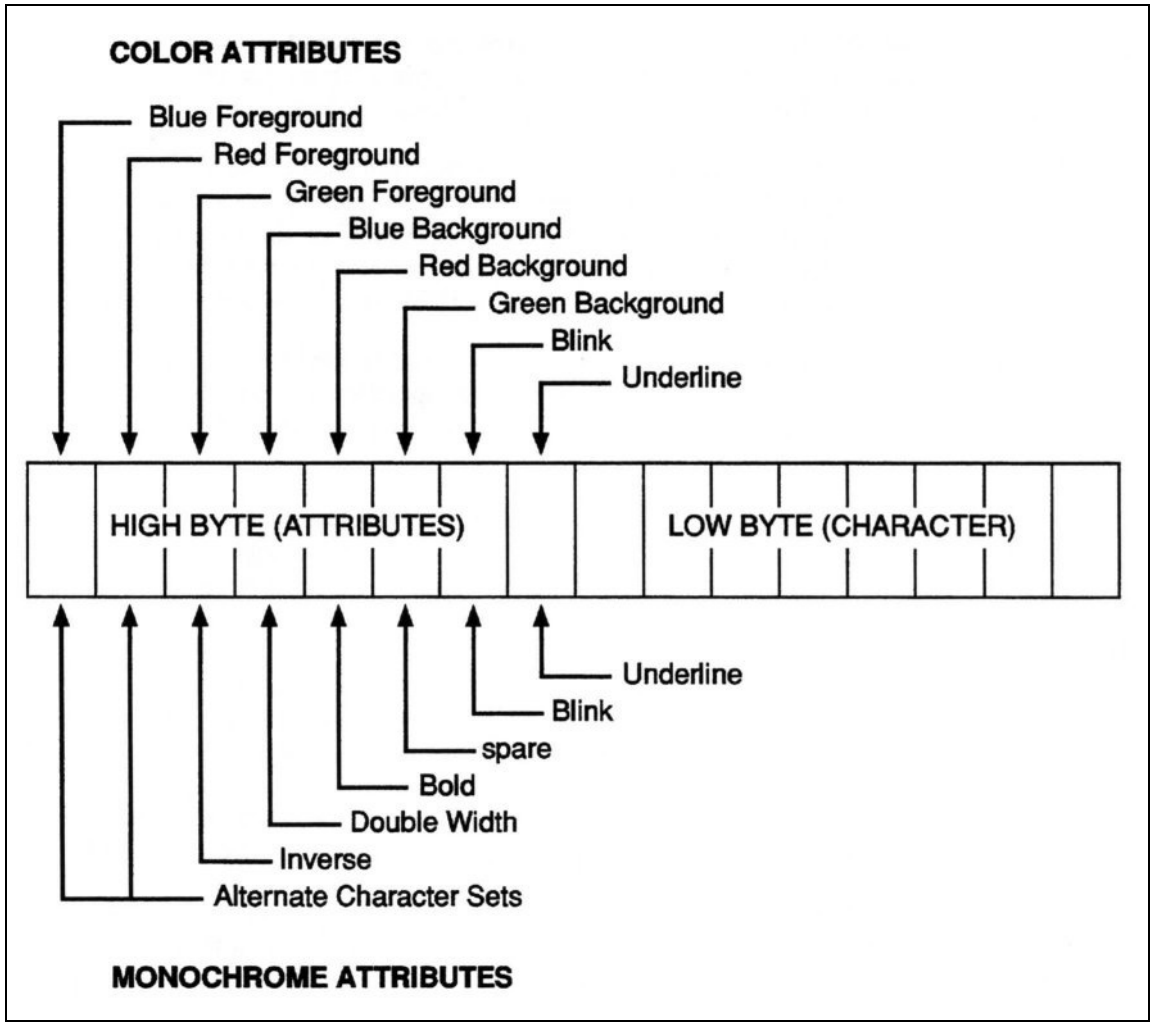


Figure 3-13. Video Character Data Format

provide high and low intensity signals. Buffer U27 sets the output voltage level, as determined by the red/blue signal intensity encoding. With a color monitor, +5V dc is provided by an earth-grounded power supply on the Main PCA. Otherwise, power from the monochrome monitor is used for enhanced noise immunity.

MONITOR 3-113.

A separate Monitor can be used with the 9100FT Video Controller. A 12-inch monochrome version is available from Fluke. This unit includes a power supply, a CRT, and CRT drive circuitry. Video timing functions are performed by the Video Controller and are not part of the Monitor.

The monitor power supply, which is not manufactured by Fluke, is a switch mode supply that operates from an unregulated 90 to 132V or 180 to 264V ac line voltage and generates the following regulated voltages:

- +12V dc ± 5%
- -12V dc ± 10%
- +5.0V dc to +5.1V dc

A color monitor can also be used. See “Color Monitor Specifications” in Section 2 for either the Fluke monochrome monitor or color monitor specifications.

PROGRAMMER’S KEYBOARD 3-114.

The Programmer’s Keyboard is a full ASCII keyboard with additional cursor control and special function keys. Key press codes are sent at 1200 baud in a standard asynchronous format of one start bit, eight data bits (LSB to MSB), and two stop bits. The keyboard buffers up to 31 key codes, at which time the buffer will be filled and subsequent key presses are lost.

The Programmer's Keyboard attaches to the ASCII Keyboard Connector (J15) on the Main PCA. A DUART-Timer-I/O (DTIO#2), U7, provides the Main PCA interface for keyboard signals. The ASCII characters are received as the RxDA input at U7-35.

PARALLEL I/O MODULE 3-115.

Parallel I/O Module Overview 3-116.

NOTE

For information on the Vector Output I/O Module (Option -017), refer to the separate Vector Output I/O Module Service Manual (P/N 855531).

The Parallel I/O Module (9100A-003) is a device that adds multiple lines of input/output capability to the 9100FT/9105FT mainframe. The Parallel I/O Module has the capability to take CRCs, measure frequency or take event counts, and record logic levels. These measurements can be done simultaneously on up to 40 lines per Parallel I/O Module. It is also possible to synchronize the data gathering to the 9100FT/9105FT uP Pod or to external events using the Parallel I/O Module external clock, enable, start, and stop lines. In addition, the Parallel I/O Module has the ability to “overdrive” dynamic patterns or static levels onto any of its lines for use in testing devices that cannot be stimulated by the uP Pod. The Parallel I/O Module is capable of reading or writing a 40-bit word, and it provides breakpoint capability by generating an interrupt when the data on the inputs equals a programmed value. Input thresholds for each module are selectable between “TTL” and “CMOS” levels. Up to four Parallel I/O Modules may be connected to the 9100FT/9105FT mainframe. The Parallel I/O Module consists of seven functional blocks. See Figure 3-14 for a functional block diagram of the Parallel I/O Module.

Each of these blocks is described in more detail in the paragraphs that follow:

- Bus Interface Functional Block
- Custom Chip Functional Block
- Clock and Enable Mux Functional Block
- General Control Latch Functional Block
- Connector Code Determination Block
- Input Protection/FET Output Block

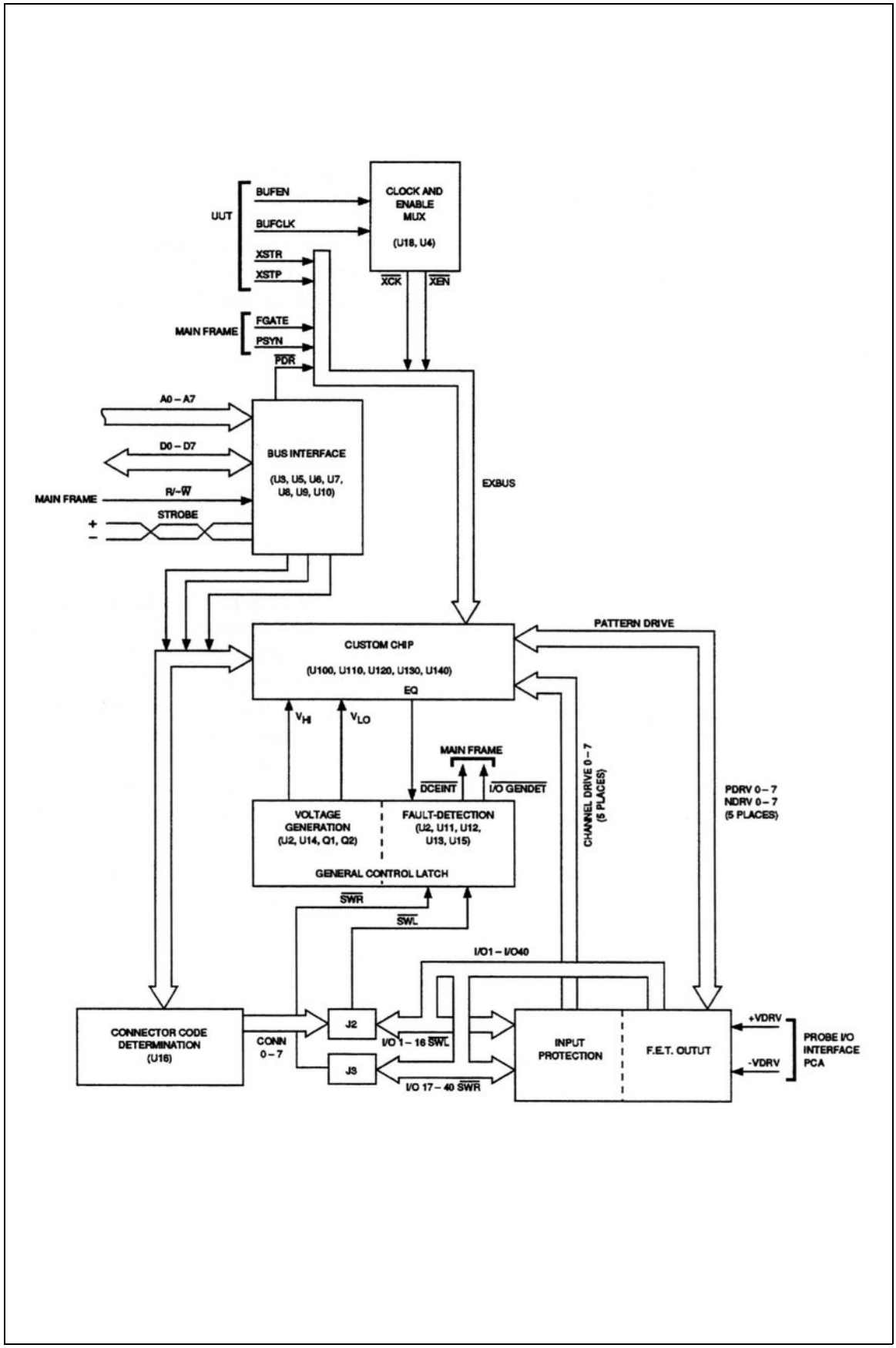


Figure 3-14. Parallel I/O Module Functional Block Diagram

Bus Interface Functional Block 3-117.

OVERVIEW 3-118.

The bus interface block connects the 9100FT/9105FT microprocessor bus to the Parallel I/O Module. The I/O Module is a memory-mapped device, with all control performed by writes to the I/O Module memory space. A control bus enters the I/O Module on connector J1 and consists of the following lines:

- Seven address lines: A01 through A07
- Eight data lines: D00 through D07
- Two differential strobe lines: STROBE+, STROBE-
- One control line: R/W-

The two strobe signals, which are sent up the cable on a twisted-pair as differential ECL signals, are the key to the clean bus interface. They are translated by U9 into the STROBE- signal. As sent by the mainframe, the STROBE- signal already has some amount of address decoding done in it; STROBE- for any particular module will only be active on byte accesses to addresses DXXXX, with internal address bit 0 = 1, and with the proper “hot bit” identifying the module. (See the paragraphs on addresses for more information on hot-bit decoding). STROBE- is the key signal used to qualify all of the bus activities and is used by U7 to latch the addresses and R/W- and to enable the data bus buffer. The STROBE- signal, in conjunction with the latched version of R/W- generates the read strobe (RD-) and the write strobe (WR-). The STROBE- signal and the decoder U6 generate the chip select signals: CS0 through CS4, ADD-, and ADE-.

The following paragraphs explain how the I/O Module address is broken down and what the hex digits signify. I/O Module selection is described with a figure showing which I/O Module(s) are selected. A timing diagram shows typical waveforms during a read and write cycle. The process of enabling the I/O Module custom chip(s) is also described.

ADDRESSING 3-119.

Memory reserved for I/O Module control occupies addresses D0000 through DFFFF. Out of this 64K-byte block, four I/O Modules can be addressed. Lower Data Strobe, (LDS-), is used to qualify all I/O Module addresses; thus address bit 0 is effectively a 1. Addresses within this space using Upper Data Strobe (UDS-) are unused. Figure 3-15 shows a summary of I/O Module address decoding. Figure 3-16 provides an addressing example.

Each of the four I/O Modules is controlled via “hot-bit decoding” of address lines A8 through A11. This method of decoding allows any combination of modules to be addressed simultaneously. A brief explanation of “hot-bit decoding” requires examination of the 5-digit hex I/O Module address. The third LSD of the address is broken down into binary form. The position of the set bit(s) determines the module(s) to be addressed. See Figure 3-17 for examples.

The timing diagram, Figure 3-18, shows the signals contained in the bus interface block during a read and write cycle. Each transition point is further explained.

- A: Address appears on bus, and R/W- goes high signifying a read cycle.
- B: RD- and CSx- go active. Data bus transceiver U8 turns on, pointing toward the mainframe. Addresses and R/W- are latched by U7 and are guaranteed valid.

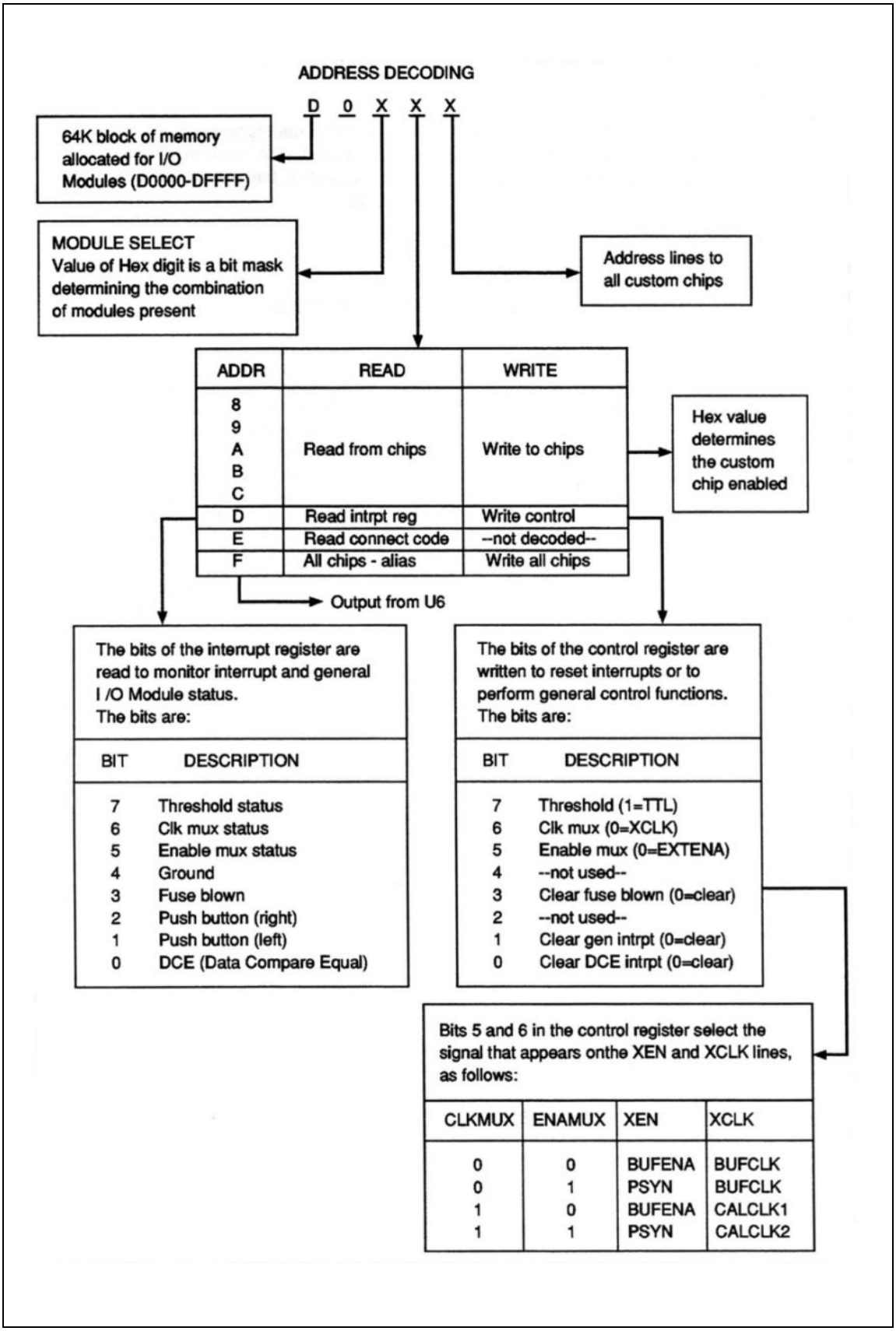


Figure 3-15. I/O Module Address Decoding Summary

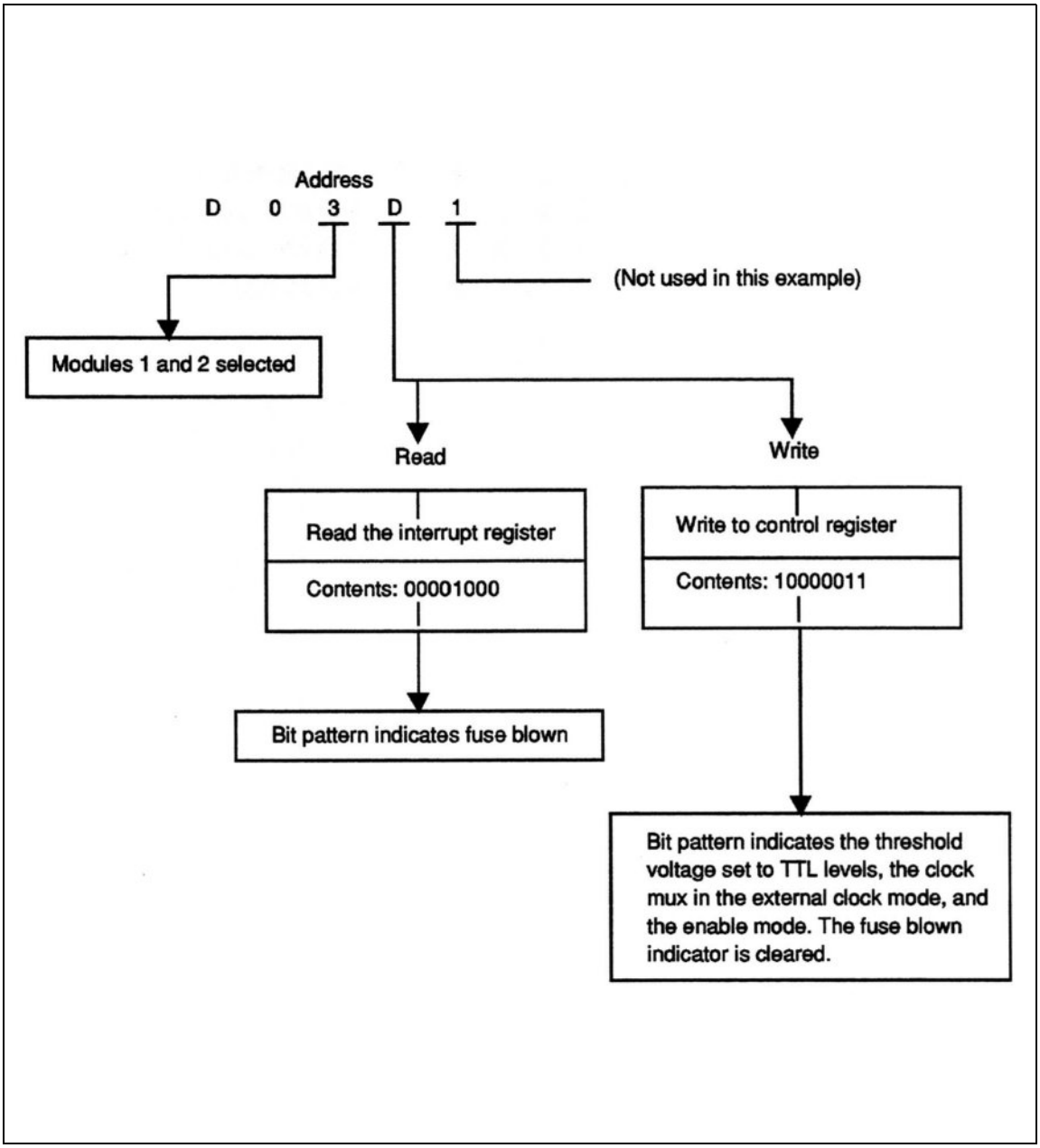


Figure 3-16. Address Decoding Example

- C: Valid read data appears on data bus.
- D: STROBE-, RD-, and CSx- return high. Read data guaranteed valid here.
- E: End of read cycle.
- F: Address appears on bus and R/W- goes low signifying a write cycle.
- G: WR- and CSx- go active. Data bus transceiver U8 turns on, pointing toward the I/O Module. Addresses and R/W- are latched and guaranteed valid.
- H: STROBE-, WR-, and CSx- return high. Write data latched into I/O Module registers.
- I: End of write cycle.

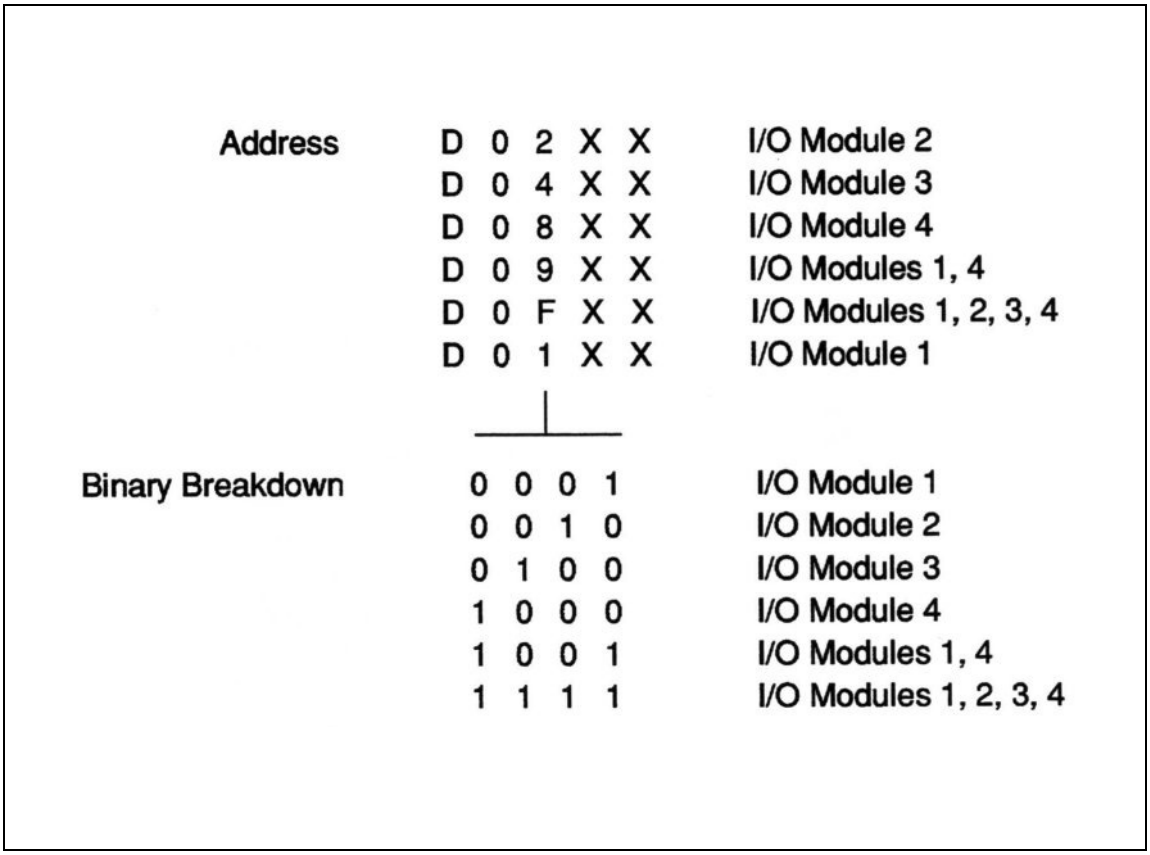


Figure 3-17. Hot-Bit Decoding Examples

CUSTOM CHIP SELECTION 3-120.

One use of the Bus Interface is to decode address lines A01 through A07 from the mainframe to determine which custom chips are enabled. As the address signals enter the Main I/O Module PCA through J1, the address lines are latched by U7 (the latch signal is STROBE-). Address lines A07 through A04 are used as address inputs for the decoder (U6). The outputs of U6 are gated to determine which custom chip is enabled. Any one of the five custom chips, or all five may be addressed simultaneously. Particular combinations of the custom chips are not addressed within a module.

For example, to select “custom chip U100”, the input at U7-13 (A07) from the address bus of the mainframe is at logic high, and U7-18 (A04), U7-17 (A05), and U7-14 (A06) are at logic low. At the occurrence of a strobe signal, U7 latches the logic levels on these pins. At the output signals of U7, LAT-A7 is logic high, and LAT-A4, LAT-A5, and LAT-A6 are logic low. U6 decodes the latched address lines and sets output line AD8- low. The logic low on AD8- is gated and sets up a logic low on CS0-, thereby enabling “custom chip U100”. If this were to occur on I/O Module 3, address D0481 would be written.

A custom chip may be addressed individually, or all custom chips may be addressed simultaneously. Address bits A04 through A07 are used to determine custom chip selection. To address all chips, an address in the form DXXFX must be used. This address causes the ALLCHIP signal (U6-7) to go active, making all five chip selects active.

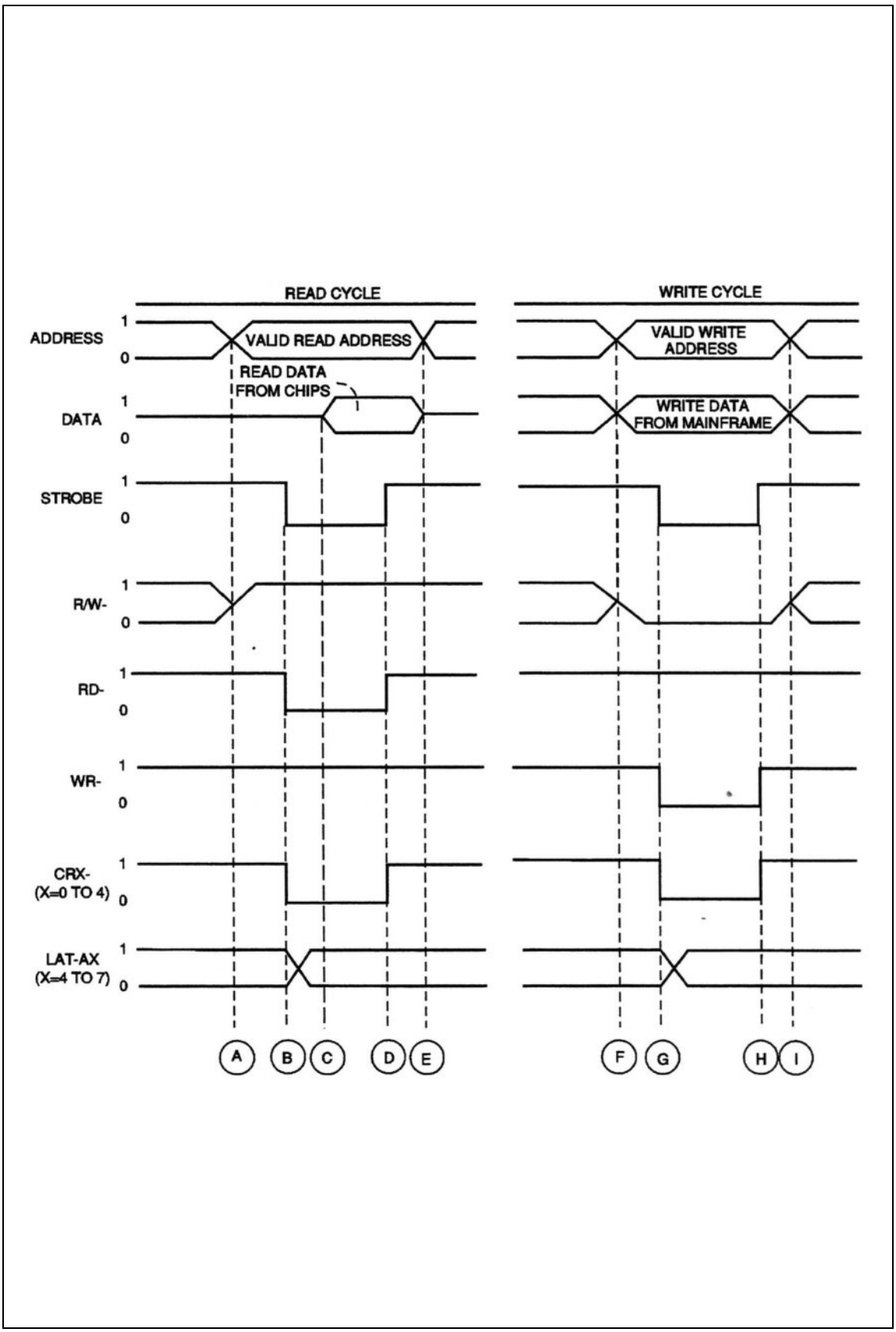


Figure 3-18. Bus Interface Timing Diagram

Table 3-26. Custom Chip Pin Description

PIN	TYPE	FUNCTION
A0-A2	Input	Address lines
POR-	Input	Power-on reset
SRCK	Input	1 MHz Serial-to-Parallel conversion clock
PDRV0-PDRV7	Output	Pattern Drive PMOS gate drive
NDRV0-NDRV7	Output	Pattern Drive NMOS gate drive
VDD1	Input	Positive voltage supply
VDD2	Input	Positive voltage supply
GND1	Input	Logic common
GND2	Input	Logic common
XDO-XD7	Input/Output	Microprocessor data bus
EQ	Output	Equal (data comparison match) output
TC	Output	Test clock output
WR-	Input	Write enable
RD-	Input	Read enable
CS-	Input	Chip select
VPAT	Input	Negative supply for DRV outputs
TEN	Input	Test mode enable
XSTP	Input	External stop
GATE	Input	Frequency gate input
XSTR	Input	External start
XEN	Input	External enable
XCK	Input	External clock
PSYN	Input	Pod sync clock
VLO	Input	Low voltage threshold select for CD0-CD7
VHI	Input	Hi voltage threshold select for CD0-CD7
CD0-CD7	Input *	Channel inputs
TLI	Input	Test channel comparator input
TLO	Output	Test channel comparator output

* CDn inputs have an internal resistor network to control the voltage at which they will float (the “invalid” voltage). This voltage is approximately 1.6V, through an effective resistance of >50 kilohms.

Custom Chip Functional Block 3-121.

The custom chips each contain eight channels of data acquisition. Each channel performs 16-bit Cyclic Redundancy Checking (CRC), 23-bit (with overflow) transition counting, 3 bits of asynchronous level history recording, 3 bits of synchronous level history recording, and 1 bit of data comparison. The custom chips are used for I/O Module control, connecting to the data bus via U8. Eleven internal registers control the custom chip. These registers are controlled by address lines A01 through A03, and the R/W- line.

The pin-out of the custom chip is shown in Table 3-26.

Clock and Enable Mux Functional Block 3-122.

The Clock and Enable Mux block is located on the I/O Module Main PCA and is shown in the I/O Module Functional Block Diagram, Figure 3-14. Two ICs make up this block: the 74HCT153 (U18) Dual 4:1 Select Multiplexer and the 74HCT04 (U4) Hex Inverter. This block selects one of three sources for the XCK- signal, and one of two sources for the XEN signal.

CLOCK AND ENABLE MUX OPERATION 3-123.

Inputs 3-124.

The Clock and Enable Mux block receives inputs from the BUFENA (Buffer Enable) and the BUFCLK (Buffer Clock) signal lines. These signal lines originate from the XCLK (External Clock) and XENA (External Enable) lines. The PSYN (Pod Sync) signal obtained from the EXT-BUS (External Bus) is an alternative clock signal to the external clock and is used for data gathering by the custom chip(s). The U18 inputs POD SYNC, CALCLK1 (Calibration Clock 1), and CALCLK2 (Calibration Clock2) are all clock signals used by the Clock and Enable Mux Block. The POD SYNC signal, which enters the I/O Module as differential ECL, is converted by U9 into TTL levels. This signal enters the EXT-BUS to be used in conjunction with CALCLK1, CALCLK2, ENMUX, and CLKMUX.

The CALCLK2 signal enters the Main I/O PCA through the Connector Code Determination Block. CALCLK 1 is not used. Channels 1 through 39 are tied together and to CALCLK 2 when the Calibration Module is plugged in. CALCLK2 is an input to U18-13. The ENMUX and CLKMUX signals are generated by the Control Register (U14-15 and U14-16, respectively) and are control inputs to U18. U18 generates outputs XEN and XCK. Table 3-27 shows which signals appear on the outputs of the multiplexer for all four states of the control inputs.

Outputs 3-125.

The Clock and Enable MUX block outputs XEN and XCK- signals to the EXT-BUS. These two control signals are sent to each custom chip. Three parallel inverters invert the XCK signal from U18-9, ensuring a fast rise time into the relatively high capaci- tance XCK- line.

General Control Latch Functional Block 3-126.

OVERVIEW 3-127.

The General Control Latch block, located on the I/O Module Main PCA, is used to vary input thresholds, clear fault conditions, and control the Clock and Enable Multiplexer. Refer to Figure 3-14 for the block's functional relationship on the block diagram. The ICs in this block include: a 74LS273 (U14) 8-bit latch, an LM324 (U2) quad op-amp, two 2N3906 (Q1, Q2) PNP transistors, a 74LS08 (U3) quad 2-input AND gate, a 74LS30 (U15) 8-input NAND gate, and two 74LS112 (U11, U12) dual JK negative-edge-triggered flip-flops.

Table 3-27. U18 Truth Table

Control In		Outputs	
CLKMUX	**ENAMUX**	**XEN**	**XCK**
0	0	BUFENA	BUFCLK
0	1	PSYN	BUFCLK
1	0	BUFENA	CALCLK 1
1	1	PSYN	CALCLK 2

CONTROL REGISTER 3-128.

Data lines from the A-D-BUS to U14 produce DCECLR- (Data Compare Equal Clear), GENCLR- (General Clear), FUSCLR- (Fuse Clear), ENMUX (Enable Multiplex), CLKMUX (Clock Multiplex), and THRSH (Threshold) signals. U14 is accessed by a write to DXXDX, where the ADD- and WR- latch data into U14. The Control Register (U14) is cleared by a PWRUP (Power Up) signal held low by C44, ensuring a proper reset.

The J2 and J3 connectors provide the input to the General Control Latch block for detection of Clip and Calibration Modules. J2-25 and J3-6 are the input pins to a detection circuit that provides the SWRDET (the right-hand or B Switch Detect) and SWLDET (the left-hand or A Switch Detect) signals to generate an interrupt. The mainframe reads the interrupt register to determine the reason for an interrupt.

DATA COMPARISON INPUTS 3-129.

All 40 lines of the I/O Module are compared to a programmable 40-bit data register and qualified by a programmable 40-bit “don't care” register. This comparison is done inside the custom chip(s), eight lines per chip. The EQ outputs (pin 55 of the custom chip), are gated together, and, when they are all high (i.e., a comparison has been detected), an interrupt is generated.

FUSE DETECTION 3-130.

The FUSEDET (Fuse Detect) is a part of the Multi-Detection area, General Control Latch Block. A 1A slow-blow ground fuse located on the I/O Module Main PCA is used to protect the ground line. The FUSEDET signal becomes an input to the interrupt register (U13-8), along with the other detection signals.

DATA COMPARISON and GENERAL INTERRUPTS 3-131.

The General Control Latch block outputs detection and interrupt signals for any problems or special operations of the I/O Module. Also, an external DCE pin allows the user to examine the state of the I/O Module hardware.

The following two interrupts are produced by the General Control Latch block:

- DCEINT- (Data Compare Equal Interrupt)
- IOGENINT- (I/O General Interrupt)

Data Compare Equal Interrupt 3-132.

The DCEINT- is generated by the I/O Module when the programmed data compare register matches the input data. The DCEINT- signal originates from the EQ pin of each custom chip. The EQ signals are gated to form a DCE- signal. The DCE- signal triggers a J-K flip-flop to produce the DCEDET and DCEINT- signals.

I/O General Interrupt 3-133.

The IOGENINT- is an interrupt generated by the I/O Module when either push button on a clip module is pressed. The interrupt status register on the I/O Module must be read to determine the cause. In the case of a button push, two J-K flip-flops output the SWLDET (A side) and SWRDET (B side) signals. These signals are gated to produce the IOGENINT- signal.

Data Compare Equal Output Pin 3-134.

DCE output pin P1-6 can be used to trigger a logic analyzer or oscilloscope. Buffers and protection circuitry safeguard the DCE signal output.

OPERATION OF GENERAL CONTROL LATCH BLOCK 3-135.

The General Control Latch Block is divided into the following three areas:

- Threshold Voltage Generation
- Multi-Detection and Interrupt
- Fuse Blown Detection

These areas produce voltages for I/O Module operation and contain circuitry that generates detection for a blown fuse.

Threshold Voltage Generation 3-136.

Threshold Voltage Generation produces the threshold voltages necessary for control of data input to the custom chips. Data Bit 7 of the command register (U14) determines the level of threshold, with a 1 selecting TTL, and a 0 for CMOS. See Figure 3-19 for the command register bit positions.

The threshold (THRSH) signal output of U14-19 passes through circuitry that produces low voltage (VLO) and high voltage (VHI) levels. These voltage levels are used by the custom chips pins 39 and 45 to define the logic low, invalid, and logic high voltage ranges. A logic high out U14-19 designates a TTL logic level; a logic low designates a CMOS level. The THRSH signal controls resistor dividers that are used to create the VHI and VHO signals. Two parts of op amp U2 and transistors Q1 and Q2 are used together to provide a regulated output with high current sinking capability. Typical current seen by these regulators can vary from 10 to 40 mA. Approximate VHI and VLO levels generated are listed in Table 3-28.

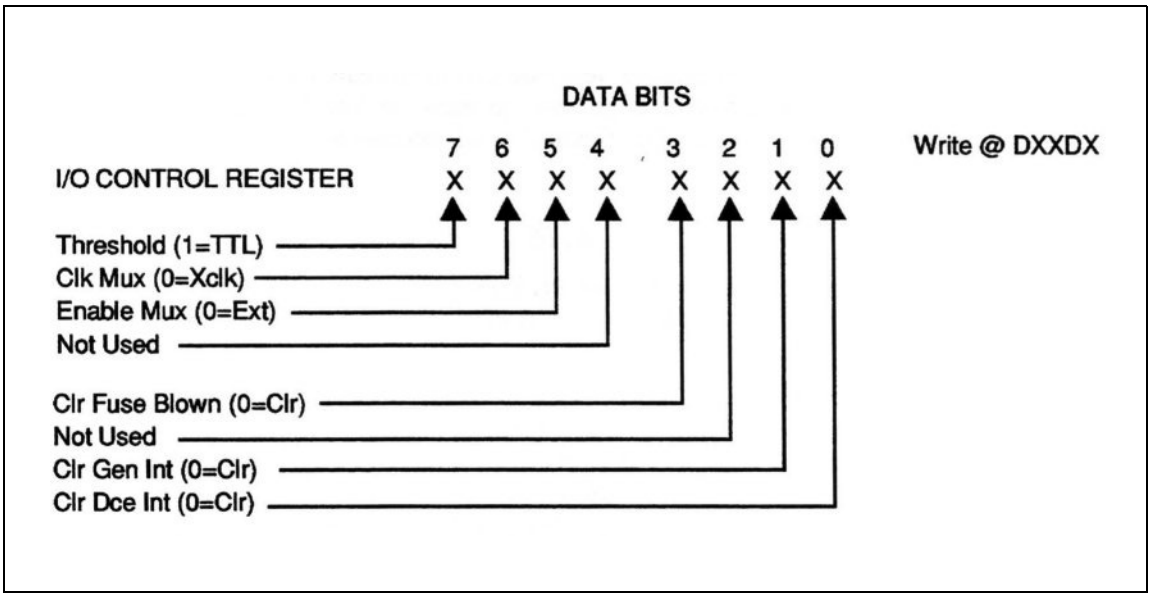


Figure 3-19. \I/O Module Command Register

Table 3-28. VHI and VLO for TTL and CMOS Logic Levels

DESC	THRSH	VHI	VLO
TTL	1	-1.0V	-2.4V
CMOS	0	-0.25V	-2.2V

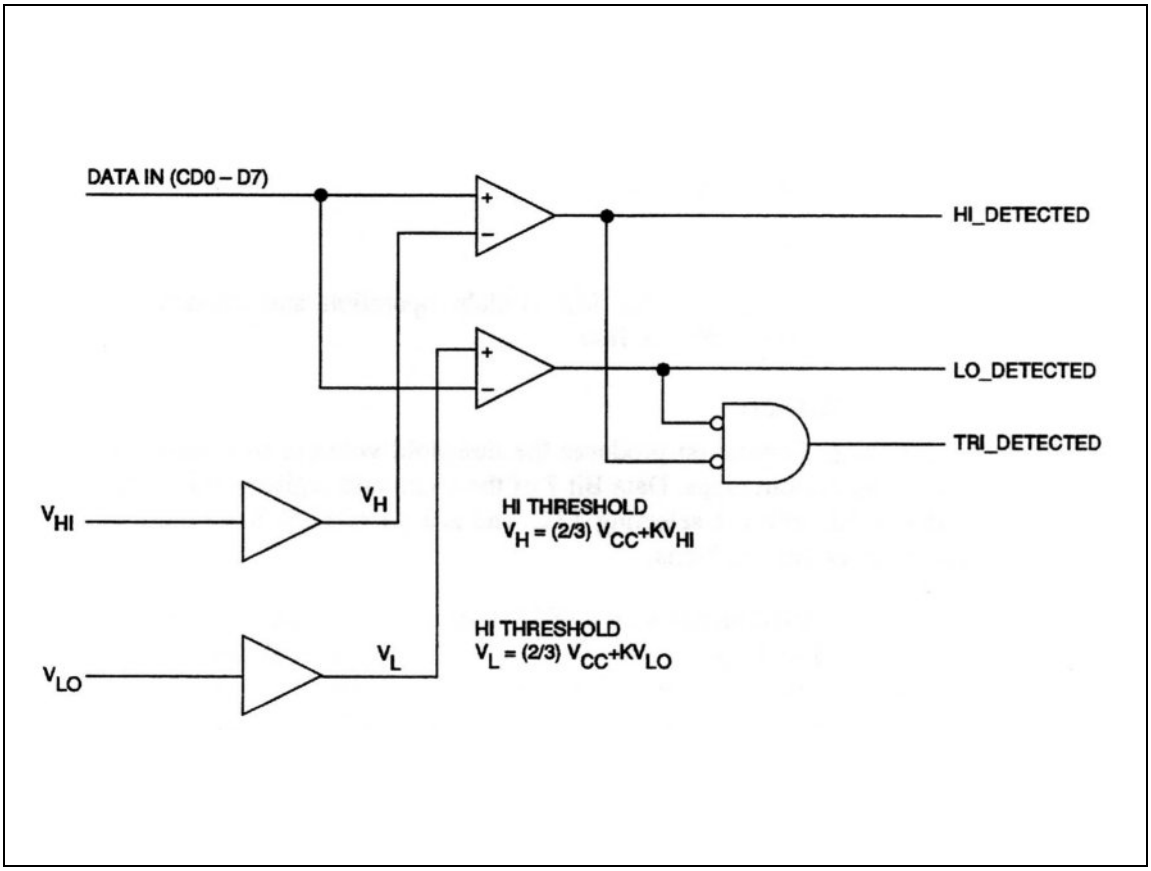


Figure 3-20. Custom Chip Voltage Level Detection

Within the custom chip, a voltage level-detection system uses data inputs, VHI, and VLO voltage levels to detect a high voltage input, a low voltage input, or a tristate situation. See Figure 3-20 for an illustration of detection circuitry within the custom chip.

NOTE

The actual input thresholds for the high and low comparators are computed from the formulas shown in Figure 3-20.

Multi-Detection and Interrupt 3-137.

The I/O Module accepts different sizes of clip modules. A detection system within the I/O Module is necessary for the mainframe to know the size of the clip that has been installed on the I/O Module. Clip Modules are available in a half-size module and a full-size module. The half-size module plugs into one connector (either J2 or J3), and the full-size module plugs into both connectors (both J2 and J3). Together, clips plugged into both J2 and J3 generate an 8-bit code that can be decoded by the mainframe to identify the plugged-in clip(s).

Fuse Blown Detection 3-138.

Detection of blown fuses is performed by two LM324 (U2) op-amps and one part of U3, configured as a window detector. If the XGND signal exceeds a ±100 millivolt window, U3-6 goes low, forcing the FUSEDET line to go high. When the Interrupt Register is read (READ @ DXXDX), a 1 in bit 3 indicates the fuse is blown. This blown fuse

indication is cleared by writing to the I/O Command Register (WRITE @ DXXDX) with a data value having bit 3 = 0.

Connector Code Functional Block 3-139.

The components associated with the Connector Code block are the 74HCT244 (U16) Octal buffer/line driver and part of J2 and J3 connectors. This block is located on the I/O Module Main PCA as indicated on function block diagram Figure 3-14.

Table 3-29. Dip-Clip and Calibration Module Configuration Codes

4 BIT CODE	MEANING
0000	14-Pin Clip
0001	16-Pin Clip
0010	18-Pin Clip
0011	20-Pin Clip
0100	24-Pin Clip
0101	(reserved)
0110	Used as most significant byte of calibration header
0111	(reserved)
1000	(reserved)
1001	(reserved)
1010	(reserved)
1100	(reserved)
1101	20-Pin Flying Lead Set
1110	Full width connector, use other 4 bits for ID
1111	No Clip Installed
8 BIT CODE 7654 3210	**MEANING**
1110 0000	28-Pin Clip
1110 0001	40-Pin Clip
1110 0010	Calibration Header
0110 0010	Calibration Header
1110 0011	(reserved)
1110 0100	(reserved)
1110 0101	(reserved)
1110 0110	(reserved)
1110 0111	(reserved)
1110 1000	(reserved)
1110 1001	(reserved)
1110 1010	(reserved)
1110 1011	(reserved)
1110 1100	(reserved)
1110 1101	(reserved)
1110 1111	(reserved)
1111 1111	No Clips Installed

Table 3-30. Connector Codes

DATA READ	MEANING
F3	No clip on B side, 20 pin clip on A side
4F	24 pin clip on B side, no clip on A side
E1	40 pin clip installed
14	16 pin clip on B side, 24 pin clip on A side
FF	no clips installed

The mainframe determines which Clip Module the user has installed by reading and decoding connector codes embedded in each Clip Module. To read the code, the mainframe performs a read @ DXXE1. This operation generates the ADE- signal, which in turn enables U16, placing the code on the data bus. Of the eight bits read, the lower four bits refer to the "A side", and the upper four bits refer to the "B side". Thus, differentiation is possible for 16 different conditions on each side of the module. Clips that use up an entire module use an 8-bit code. The most significant nibble of these codes is 1110. For a list of the codes, see Table 3-29.

CONNECTOR CODE EXAMPLES 3-140.

If the connector codes are to be determined on I/O Module 3, a Read @ D04E1 (byte mode) would be performed. Table 3-30 presents some examples of codes and their interpretation.

Input Protection/FET Output Block 3-141.

OVERVIEW 3-142.

The Input Protection/FET Output Block combines the functions of input channel protection for each custom chip and output for the Parallel I/OModule. Input protection

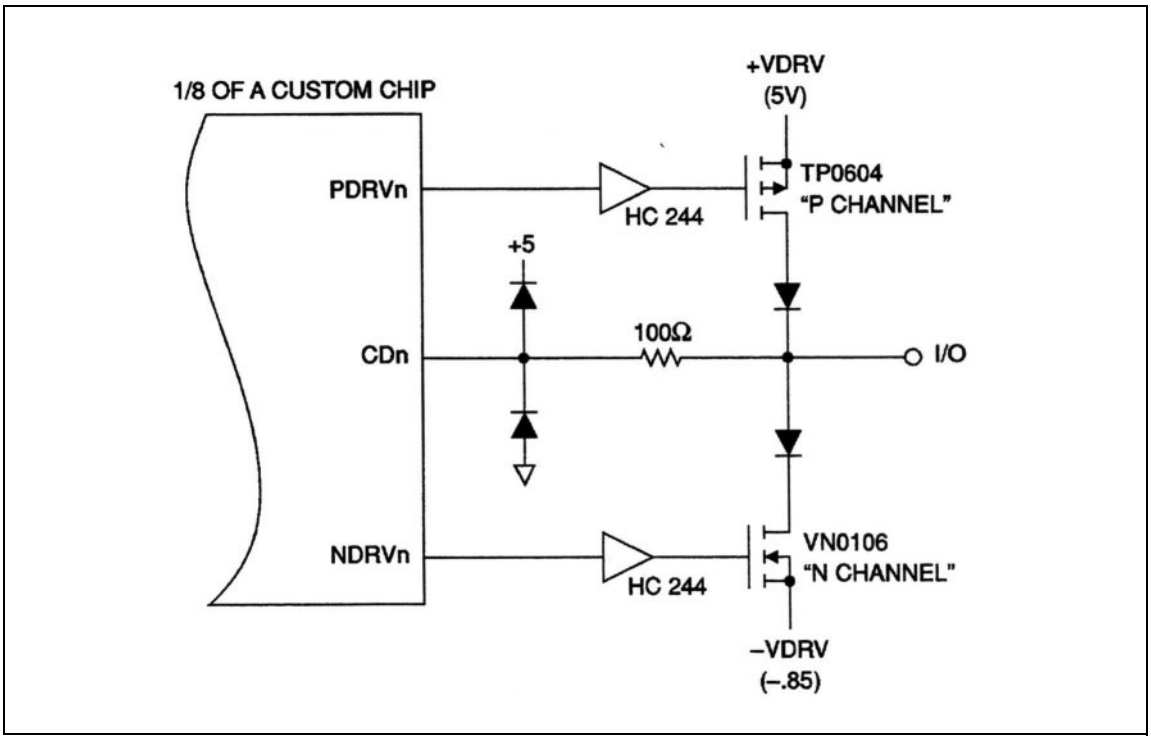


Figure 3-21. Chip Channel Input/Pattern Drive Output Simplified Schematic

clamps overvoltage, undervoltage, and static conditions before they reach the custom chip.

The output circuitry uses complementary N and P channel DMOS FETs. These FETs can be commanded to drive the I/O line high or low or leave it undriven (off). The custom chip drives these FETs through a 74HC244 buffer. Figure 3-21 shows a simplified circuit of a single channel. All 40 channels are functionally identical to each other.

This output circuit uses power supplies +VDRV (+5V dc) and -VDRV (-0.85V dc). These voltages are generated, regulated, and current-limited on the Probe I/O-ECL and I/O Connector PCAs.

INPUT PROTECTION SECTION OPERATION 3-143.

Data from the I/O lines travels through its respective connector into the protection circuit. Diodes (connected to +5V dc and ground) protect the custom chip from undervoltage and overvoltage.

FET OUTPUT SECTION OPERATION 3-144.

The output block can assume three states: high, low, and off. The output block, in conjunction with the input block, allows for measurement of signals at the inputs. The truth table shown in Table 3-31 lists the logic levels of NDRV and PDRV.

Parallel I/O Module Top PCA Functional Block 3-145.

The top pca of the Parallel I/O Module is a four-layer board consisting of connectors J2 and J3, banana plugs P1-P4, headers J1 and J4, and four 4700-µF capacitors. The top board connectors (J2, J3) provide the input for the 40 I/O lines from the Clip or Calibration Module. The four capacitors together form an effective 4700-µF bipolar capacitor. This is placed across the ground fuse to lower the fuse impedance. P1-P4 represent reference plug-in points between the plug-in Clip Module and the Parallel I/O Module for external ground and signal ground. The top Parallel I/O Module PCA allows for plug-in of a half or full Clip Module or a Calibration Module.

These modules plug into J2 and/or J3 of the top PCA and transfer I/O lines to J2 and J3 of the Parallel I/O Module Main PCA. P1 and P3 are the signal ground connection points between the Parallel I/O Module and the Clip Module. P2 and P4 are the external ground connection points. These connection points improve grounding by providing multiple paths between the clip modules and the Parallel I/O Module.

CLIP AND CALIBRATION MODULE FUNCTIONAL BLOCK 3-146.

The Clip Module is a 9100FT/9105FT system accessory that offers the user a selection of configurations to test UUT I/O lines. There are two different sizes, a half width and a full width. The number of pins each size can handle is explained in the following paragraphs. The Calibration Module is another unit that the user installs onto the top of the Parallel I/O Module for calibration of clock signals.

Table 3-31. Logic Levels of NDRV and PDRV

OUTPUT	NDRV	PDRV
HI	0	0
LO	1	1
OFF	0	1
(illegal)	1	0

Overview of the Clip and Calibration Modules 3-147.

The Half-Width Clip Module is used for connecting the Parallel I/O Module to an IC. Five modules are available, in 14-, 16-, 18-, 20-, and 24-pin configurations. If one of these IC clip modules cannot be used, a 20-pin flying lead set is available.

The Full-Width Clip Module connects the Parallel I/O Module to 28- and 40-pin IC configurations. The Full Width Module contains two connectors to provide access for up to 40 I/O lines and a ribbon cable attached to either a 28- or a 40-pin IC clip.

The Calibration Module helps perform Parallel I/O Module calibration by assuring that simultaneous level transitions occur at both the clock and data inputs of the Parallel I/O Module. The clock and data inputs are recorded simultaneously by the latches in the Parallel I/O Module. The Calibration Module attaches to the two I/O Module connectors (J2, J3).

Clip and Calibration Module Operation 3-148.

HALF WIDTH CLIP MODULE 3-149.

The user plugs the Clip Module into the top of the Parallel I/O Module, then attaches the clip connected to a ribbon cable to the UUT. The Half Width Module can be connected to J2 (A side) or J3 (B side) of the Parallel I/O Module.

NOTE

Check the schematic for the I/O signals lines used in each case.

An SPST four-position dip switch contained in the Half-Width Module determines the code for the module. This code tells the mainframe the type of pin configuration used during the current I/O test. The connector code is factory set, and should not be changed. For a list of connector codes, see Table 3-29. A black ID button located on the front of the module housing can be used to signal the mainframe.

FULL-WIDTH CLIP MODULE 3-150.

The Full-Width Module connects to IC chips under test (28- and 40-pin configurations). The Full-Width Module uses the same procedures and tests as the Half-Width Module. The Full-Width Module uses both I/O Module connectors for the additional I/O signal lines.

To identify the connection code of the Full-Width Module, the Module contains an SPST eight-position DIP switch. The Full-Width Module requires an 8-bit connection code so that the mainframe can determine the size of the clip the user has plugged into the Parallel I/O Module. A black ID button located on the front of the Full-Width Module is used to signal the mainframe.

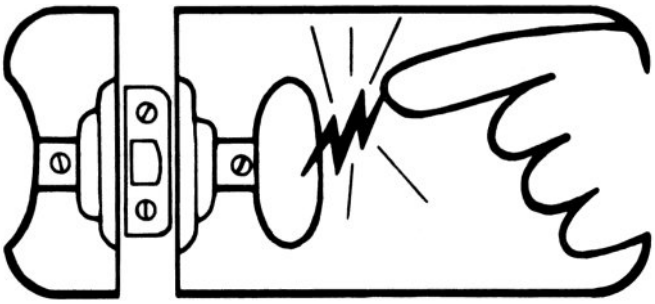
CALIBRATION MODULE 3-151.

The Calibration Module is used in calibrating both the delay between the data input and the external clock output and the delay between the data input and the pod synchronous clock. The Calibration Module ties channels 1 through 39 and CALCLK2 together. Channel 40 is connected to a “Flying Lead” and is used for calibration to the pod. With the Clock Multiplexer (U18) signal properly programmed, CALCLK2 appears on the XCK lines and clocks all of the custom chips. The Calibration Module connection code is hard-wired as Hex E2. The Calibration Module has an ID button located externally for detection by the mainframe.

static awareness

A Message From

John Fluke Mfg. Co., Inc.

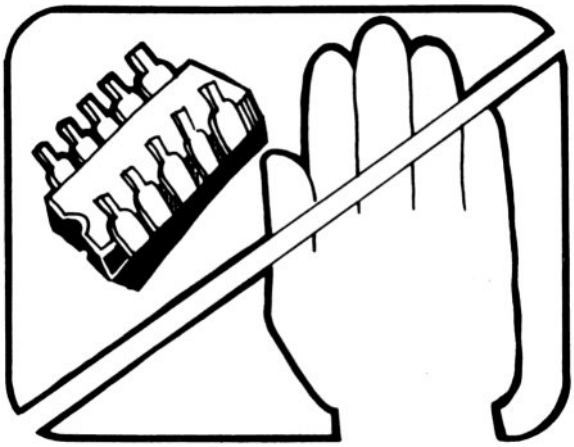


Some semiconductors and custom IC's can be damaged by electrostatic discharge during handling. This notice explains how you can minimize the chances of destroying such devices by:

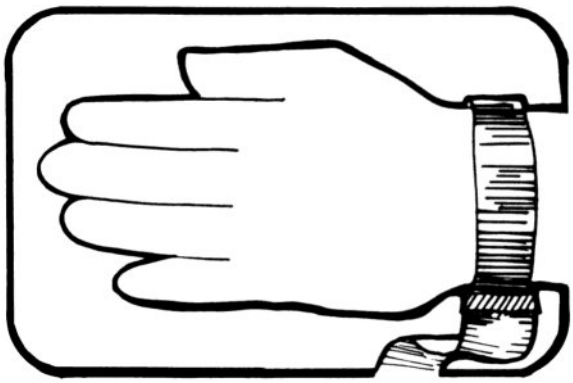
1. Knowing that there is a problem.
2. Learning the guidelines for handling them.
3. Using the procedures, and packaging and bench techniques that are recommended.

The Static Sensitive (S.S.) devices are identified in the Fluke technical manual parts list with the symbol

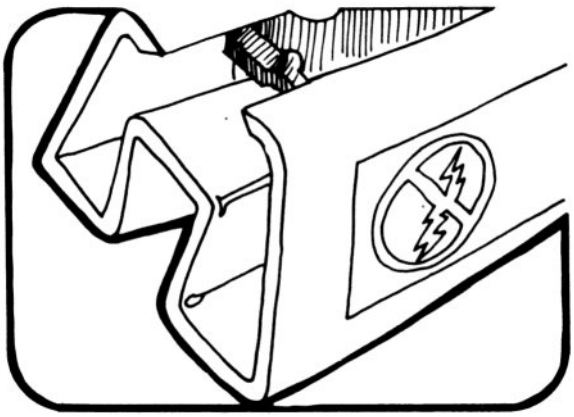
The following practices should be followed to minimize damage to S.S. devices.



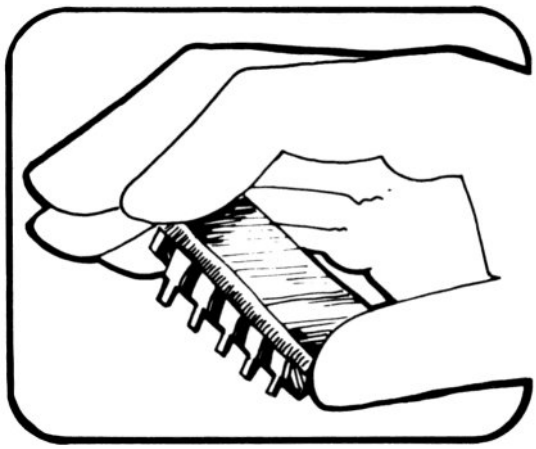
1. MINIMIZE HANDLING



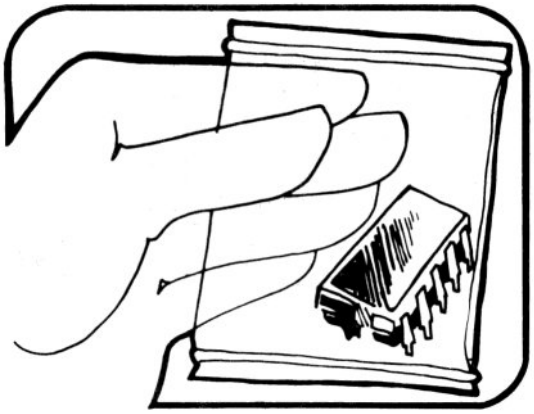
3. DISCHARGE PERSONAL STATIC BEFORE HANDLING DEVICES. USE A HIGH RESISTANCE GROUNDING WRIST STRAP



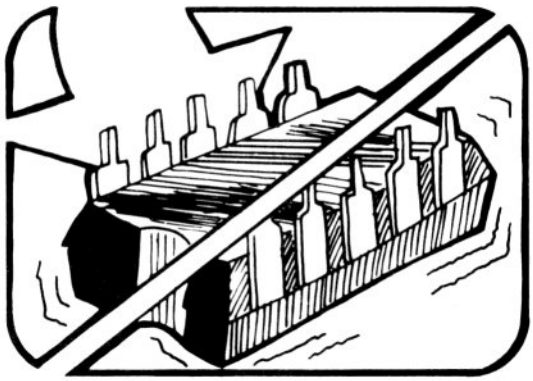
2. KEEP PARTS IN ORIGINAL CONTAINERS UNTIL READY FOR USE.



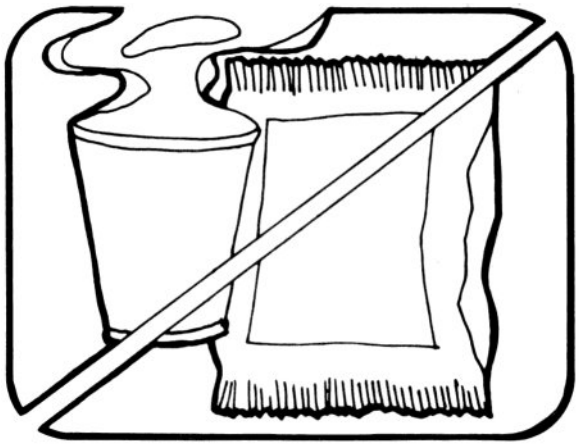
4. HANDLE S.S. DEVICES BY THE BODY



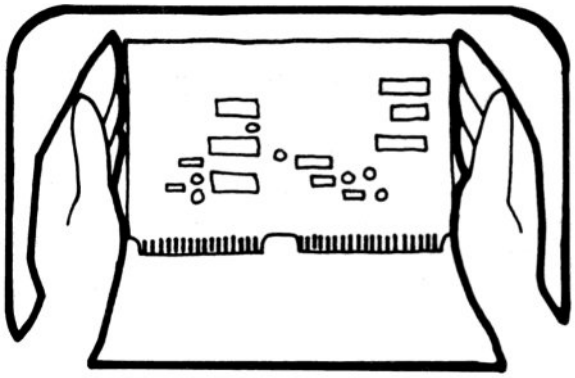
5. USE STATIC SHIELDING CONTAINERS FOR HANDLING AND TRANSPORT



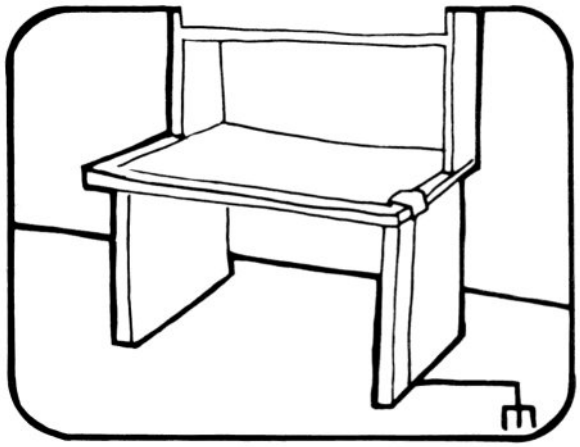
6. DO NOT SLIDE S.S. DEVICES OVER ANY SURFACE



7. AVOID PLASTIC, VINYL AND STYROFOAM® IN WORK AREA



8. WHEN REMOVING PLUG-IN ASSEMBLIES, HANDLE ONLY BY NON-CONDUCTIVE EDGES AND NEVER TOUCH OPEN EDGE CONNECTOR EXCEPT AT STATIC-FREE WORK STATION. PLACING SHORTING STRIPS ON EDGE CONNECTOR HELPS TO PROTECT INSTALLED SS DEVICES.



9. HANDLE S.S. DEVICES ONLY AT A STATIC-FREE WORK STATION
10. ONLY ANTI-STATIC TYPE SOLDER-SUCKERS SHOULD BE USED.
11. ONLY GROUNDED TIP SOLDERING IRONS SHOULD BE USED.

A complete line of static shielding bags and accessories is available from Fluke Parts Department, Telephone 800-526-4731 or write to:

JOHN FLUKE MFG. CO., INC.
PARTS DEPT. M/S 86
9028 EVERGREEN WAY
EVERETT, WA 98204

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Section 4
Maintenance

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WARNING

SERVICING DESCRIBED IN THIS SECTION IS TO BE PERFORMED BY QUALIFIED SERVICE PERSONNEL ONLY. TO AVOID ELECTRICAL SHOCK, DO NOT PERFORM ANY SERVICING UNLESS YOU ARE QUALIFIED TO DO SO.

INTRODUCTION 4-1.

This section describes maintenance procedures for the 9100FT/9105FT. Some of these procedures do not require access to the instrument and can be performed by the operator. Troubleshooting procedures, which are covered in detail in the 9100FT/9105FT Service Kit, may require reference to the disassembly and reassembly instructions found in this section.

Refer to Table 2-2 for a list of tools and test equipment required during 9100FT/9105FT maintenance.

SELECTING LINE VOLTAGE 4-2.

Selecting Mainframe Line Voltage 4-3.

The mainframe line voltage selection switch is located on the 9100FT/9105FT rear panel. The switch setting (110V or 220V) must correspond to the local line voltage as follows:

Setting	Voltage/Frequency Range	Required Fuse (F1)
110V	90 to 132V ac, 47 to 440 Hz	2A SLOW BLOW
220V	180 to 264V ac, 47 to 63 Hz	1A SLOW BLOW

A correct setting can be verified visually at any time. Otherwise, to change the setting, use the following procedure:

1. Ensure that the 9100FT/9105FT is turned off and its line power cord is disconnected.
2. Rotate the rear panel switch to the desired setting (110V or 220V).
3. If necessary, replace the power fuse as described later in this section. See Table 4-1 for the fuse part number.
4. Connect the power cord to the correct line voltage, and turn the 9100FT/9105FT on.

Selecting Monitor Line Voltage 4-4.

The line voltage selection switch for the Fluke Monochrome Monitor is located on the monitor rear panel. The mainframe voltage setting (110V or 220V) must be repeated with the Monitor. No fuse changes are required with monitor line voltage changes.

Setting	Voltage/Frequency Range
110V	90 to 132V ac, 47 to 440 Hz
220V	180 to 264V ac, 47 to 440 Hz

To change the setting, use the following procedure:

1. Set the rear panel power switch to off (“0”).
2. Rotate the rear panel switch to the desired setting (110V or 220V).
3. Connect the power cord to the correct line voltage, and set the power switch to on (“1”)

CHANGING FUSES 4-5.

Changing the Mainframe Fuse 4-6.

The mainframe fuse (labeled F1) is accessible from the rear panel. Prior to changing the fuse, set power to off and remove the line power cord. Then, press in and turn the fuse holder cap counterclockwise. Fuse sizes are:

110V	2A SLOW BLOW
220V	1A SLOW BLOW

See Table 4-1 for fuse part numbers.

Changing the Probe Fuse 4-7.

An operator display message (“probe fuse blown”) indicates that the probe fuse has opened. This problem can occur when the probe common lead is incorrectly connected to the UUT.

Prior to replacing the fuse, determine the incorrect common lead connection. Then disconnect probe leads and replace the fuse as follows:

1. Locate the fuse holder, labeled PROBE FUSE, on the mainframe right side.
2. Press the fuse holder cap in, then rotate it counterclockwise.
3. Pull the cap and fuse straight out. Separate the fuse cap and fuse.
4. Use a 0.25A, 250V fast-blow fuse. See Table 4-1 for the fuse part number.

Changing the Clock Module Fuse 4-8.

An operator display message (“clock module fuse blown”) indicates that the Clock Module fuse has opened. This problem can occur when the Clock Module COMMON lead is incorrectly connected to the UUT.

Prior to replacing the fuse, determine the incorrect COMMON lead connection. Then disconnect all Clock Module leads and replace the fuse as follows:

1. Locate the fuse holder on the Clock Module.
2. Press the fuse holder cap in, then rotate it counterclockwise.
3. Pull the cap and fuse straight out. Separate the cap and fuse.
4. Use a 0.25A, 250V fast-blow fuse. See Table 4-1 for the fuse part number.

Changing the I/O Module Fuse 4-9.

An operator display message (“I/O module fuse blown”) indicates that the I/O Module fuse has opened. This problem can occur when the I/O Module COMMON lead is incorrectly connected to the UUT.

Prior to replacing the fuse, determine the incorrect COMMON lead connection. Then disconnect all I/O Module leads and replace the fuse as follows:

1. Locate the fuse holder on the back of the I/O Module, near the cable.
2. Press the fuse holder cap in, then rotate it counterclockwise.
3. Pull the cap and fuse straight out. Separate the cap and fuse.
4. Use a 1A, 250V slow blow fuse. See Table 4-1 for the fuse part number.

Each 9100FT or 9105FT uses one of two different types of fuses. Instruments configured at the factory for 110V line voltage use 1/4 x 1-1/4 inch fuses with grey fuse holder caps. Instruments configured at the factory for 220V use 5 mm x 20 mm fuses with black fuse holder caps. First, check the color of the fuse cap (grey caps hold U.S. fuses; black caps hold metric fuses). Then select the fuse part number as shown in Table 4-1.

CLEANING 4-10.

General 4-11.

CAUTION

Do not use aromatic hydrocarbons (such as gasoline or other fuels) or chlorinated solvents for cleaning. They may damage plastic materials used in the instrument.

Avoid using excessive amounts of liquid, particularly around the keypad, keyboard, or disk drives.

Both the operator's display and the monitor screen should be cleaned with a soft cloth that has been lightly dampened with a cleaner. Commercially-available lens or CRT cleaners or nonabrasive household cleaners are appropriate for this purpose.

Clean the instrument exterior and accessory cables with either a mild solution of detergent and water or a nonabrasive household cleaner.

The operator's keypad and keyboard should be cleaned gently with a cloth or towel that has been lightly dampened with either a nonabrasive household cleaner or a mild solution of detergent and water.

Fan Filter 4-12.

The fan filter should be cleaned at least once every 90 days, or more often if necessary, to ensure the free flow of cooling air. The filter is positioned behind the louvered filter cover found on the mainframe right side.

To remove the filter, first pull on the cover at both sides of the upper disk drive. Once the latching pins have snapped out of the chassis, lift up on the cover until its bottom is free. Remove and clean the foam filter. Use warm water and detergent.

Floppy Disk Drive 4-13.

Each floppy disk drive should be cleaned at least once a year. Cleaning involves running a commercially-available cleaning disk in the drive for five seconds.

Table 4-1. Fuse Part Numbers

FUSE	US P/N	METRIC P/N
2A SLOW BLOW	109181	na
1A SLOW BLOW	109272	808055
0.25A FAST BLOW	109314	543504
The fuse holder cap is part number 460238 for U.S (grey) usage and 461020 for metric (black) usage.		

MAINFRAME ACCESS, REMOVAL, AND INSTALLATION TECHNIQUES 4-14.

System Connections 4-15.

System connections are fully explained in the Getting Started guide. Here, in the Service Manual, Figures 4-1 and 4-2 also illustrate system component interconnections. If additional information about reconnecting the system is needed, refer to the Getting Started Guide.

Mainframe Access 4-16.

WARNING

TO REDUCE THE RISK OF ELECTRIC SHOCK ALWAYS TURN OFF THE 9100FT/9105FT AND DISCONNECT THE POWER CORD FROM THE PANEL ON THE REAR OF THE CHASSIS BEFORE ACCESSING THE MAINFRAME.

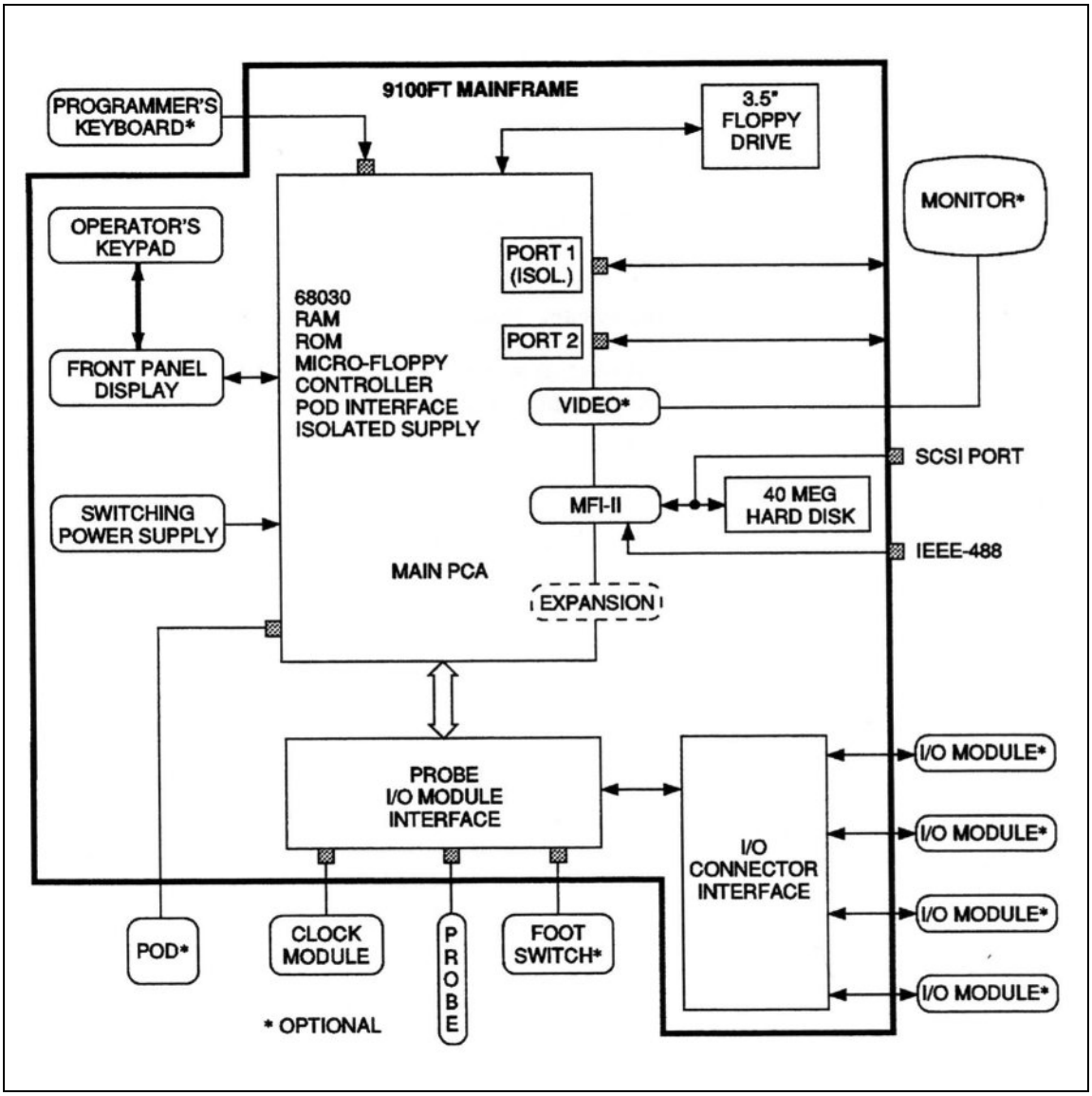


Figure 4-1. 9100FT System (with Programmer's Station)

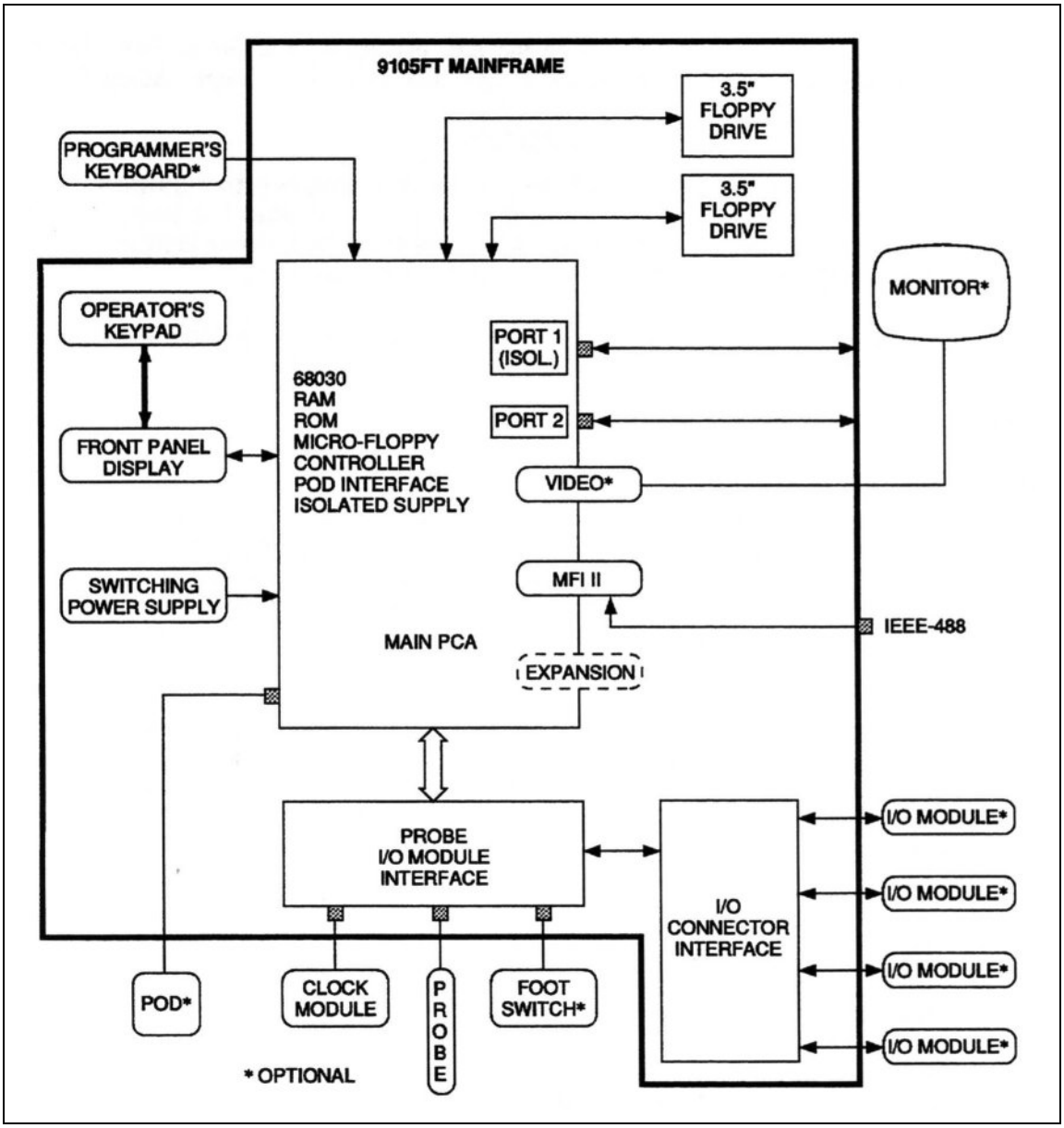


Figure 4-2. 9105FT System

1. With the instrument positioned bottom side up, remove the five screws securing the top. There are two screws on each of the side lips and one screw located at the bottom front.

2. Holding case top and bottom together, rotate the entire instrument to the top up position.

3. Working from the front of the instrument, remove the top cover by gently lifting at midpoint on both sides.

NOTE

Once the cover is free of the mainframe, notice the various cables attached between it and the mainframe. Protect these cables by proceeding cautiously with the following steps.

4. Rotate the cover 90 degrees clockwise.

5. Tilt the top cover 90 degrees to the left, placing it on a flat surface next to the mainframe. In this position, the floppy disk drive is on edge, facing forward.

CAUTION

The floppy disk drive must be positioned properly to function reliably. Do not position the removed cover so that the floppy disk drive is on top, facing up. Also, the hard disk drive (9100FT only) may fail if operated in an incorrect position.

Any instrument assembly or subassembly can now be removed. Note that removal of some assemblies requires prior removal of other assemblies.

Operator Keypad/Display 4-17.

REMOVING THE ASSEMBLY 4-17.

The Keypad/Display is attached to the mainframe electrically with one ribbon cable and is physically attached with two screws. First, disconnect the cable at either end (J10 on the Main PCA, or J1 on the Display Interface PCA) by grasping the connector and pulling with a gentle end-to-end rocking action, Then remove the two side screws (one at each pivot point), and pull the Keypad/Display free of the mainframe.

SEPARATING THE SUBASSEMBLY 4-18.

The Keypad and Display can be separated by first disconnecting the ribbon cable connector at J2 (Display Interface PCA). Grasp the connector at both ends and pull with a gentle end-to-end rocking action. Then remove the two securing screws, one at each corner of the pca case. Finally, while guiding the ribbon cable and connector through the respective pca opening, pull the Keypad and Display subassemblies apart.

NOTE

On the Keypad, the two round rotator caps are no longer secured in place when the subassemblies are detached. These caps should be retained separately to avoid inadvertent loss.

When reconnecting the Keypad and Display subassemblies, route the ribbon cable/connector back through the pca opening, but avoid actual connection to the pca until the two securing screws are tightened. This sequence avoids undue stress on the cable and connector.

DISASSEMBLING THE KEYPAD 4-19.

Although Keypad disassembly is seldom necessary, it can be accomplished quite easily. Before beginning disassembly, awareness of the two precautions is important.

- Once the keypad halves are separated, the keys are no longer secured in place. Avoid key loss by separating the keypad and case only when the keypad is upside down (keys facing down).

- Each rotator cap conceals a spring and plastic securing flange. Particularly note the flange orientation; a small “R” faces right, and a small “L” faces left. Each flange must be reinstalled in the same manner. Also, the springs are not secured in place once the keypad halves are separated and must be separately retained. When separating the keypad halves, note the location of the alignment holes used by the springs.

Use the following steps to separate the two keypad case halves:

1. Remove the screw found along the rear of the keypad.
2. Turn the keypad so that the keys face down, then pull off the securing flange revealed under each rotator cap. Note the orientation of the torsion springs (one at each end).
3. Now pry the two case halves apart, and remove the torsion springs. Leave the key half facing down until otherwise called for during reassembly.

Use the following procedure to reconnect the keypad case halves.

1. With the key half still facing down, install the torsion springs in their respective alignment holes.
2. Now, while holding each spring in place, lower the bottom half onto the key half.
3. Once the springs are properly aligned, install the two securing flanges in the same orientation as noted earlier.
4. Carefully rotate the two halves so that the keys face up. Then press and secure each of the three securing tabs along the front.
5. Install the securing screw.

Disassembling the Disk System 4-21.

REMOVING THE DISK DRIVE ASSEMBLY 4-22.

Refer to Figure 4-3. In sequence, remove the 50-pin ribbon cable connector from the hard disk (9100FT only), the 34-pin ribbon cable connector at J9 (Main PCA), and the seven screws securing the disk drive assembly. Grasp the assembly securely before removing the final screw.

The disk drives can now be removed from the disk drive assembly as described below.

- Floppy Disk Drive: Remove the two screws from each side. Lift or slide the drive out. Then remove the power connector.
- Hard Disk Drive: Remove the two screws from each side. Gently slide the drive out. Then disconnect the power connector.

CAUTION

The Hard Disk Drive is extremely fragile. Do not jar this assembly at any time during installation or removal.

INSTALLING THE DISK DRIVE ASSEMBLY 4-23.

Generally, reassembling and installing the Disk Drive Assembly involves reversing the steps used above during removal. Make sure the 34-conductor ribbon cable and the 4-conductor discrete cable are not pinched between the disk drive assembly and the top cover.

Removing the Power Supply 4-24.

The Power Supply Assembly uses electrical connections to the Main PCA, the rear panel fuse and power switch, and the disk drive assemblies (as applicable). Disconnect the related cables at the Main PCA and at the in-line connector leading to the rear panel fuse/power switch.

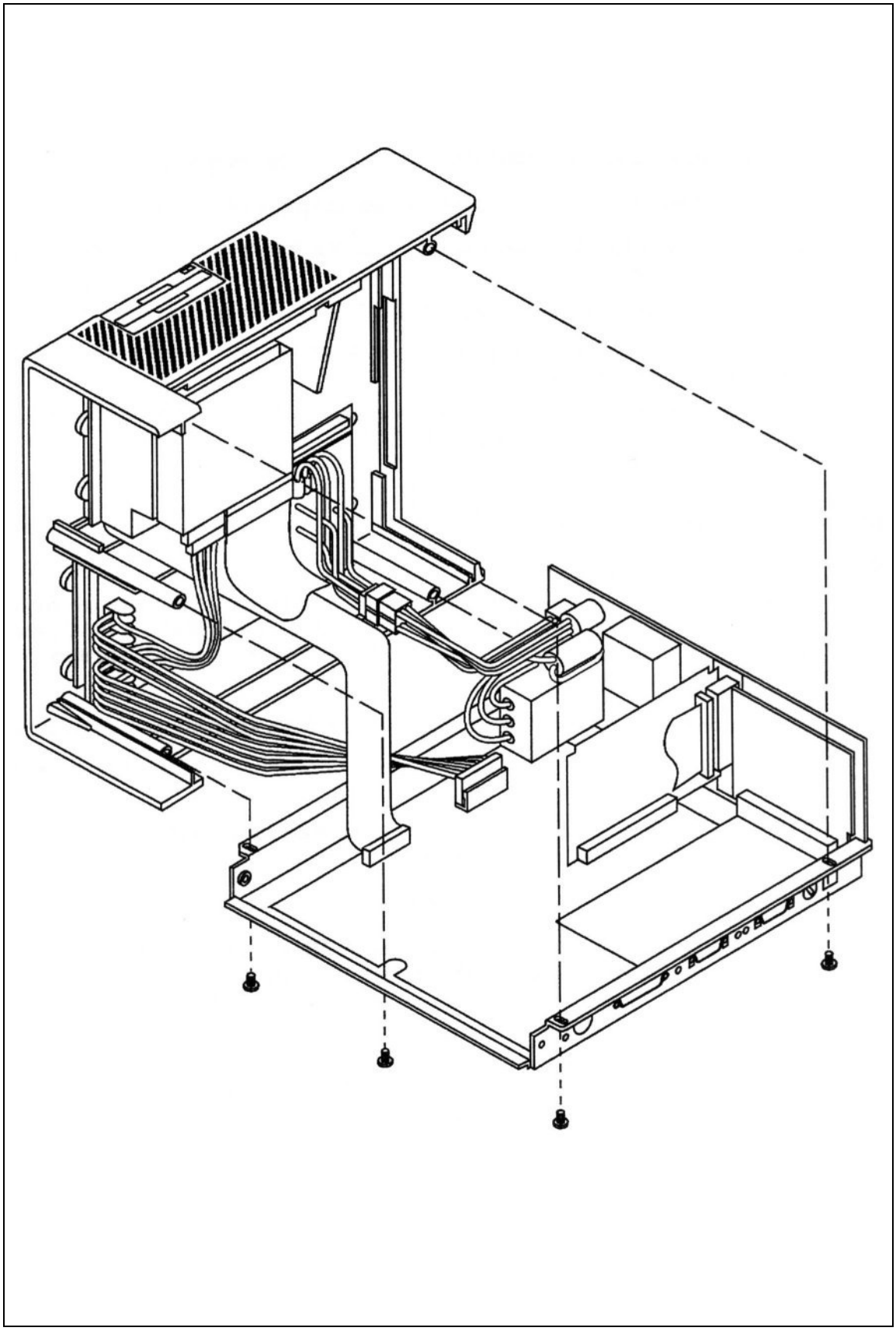


Figure 4-3. Disassembly Details

To remove the connections to the disk drives, remove the Disk Drive Assembly, and unplug the power connectors to the floppy disk drive(s) and hard disk (9100FT only). Disk drive disconnection can also be accomplished by removing the power supply wiring harness from the terminal blocks on the Power Supply Assembly.

Remove the five securing screws, and lift the Power Supply PCA free. Note that four shoulder screws (with nylon washers) are used in the corners. Make sure these items are used during reassembly.

If this Power Supply will not be reused in the same instrument, remove the back mounting plate. This plate adapts the Power Supply mounting requirements to those of the 9100FT/9105FT top cover.

Removing the MFI II and Video Controller PCAs 4-25.

Remove the Multi-Function Interface (MFI) II PCA, Video Controller PCA, or the Expansion PCA using the following procedure:

1. From the rear panel, remove the screws securing the pca.
2. To dislodge the pca from its connector, alternately lift first at the top-rear, then at the top-front.

Removing the I/O Connector Interface PCA 4-26.

Remove the three screws securing the I/O Connector Interface mounting plate to the rear panel. Then pull the mounting plate and pca straight up. The pca can be detached from its mounting plate by removing the two screws securing each of the four I/O Module connectors.

Removing the Probe I/O-ECL PCA 4-27.

1. Remove the I/O Connector Interface PCA (see above).
2. Detach the ribbon cable connectors at J6 and J7. Grasp each connector at both ends and pull with a gentle end-to-end rocking action.
3. Detach the pca connector for the rear panel TRIGGER OUTPUT.
4. On the right side of the mainframe, remove two screws each for the CLOCK MODULE connector and the PROBE connector.
5. Now remove the four screws securing the pca in place.
6. Gently lift on the inside edge until the pca is detached from the remaining clip connection to the mainframe.

Removing the Main PCA 4-28.

Use the following procedure for removing the Main PCA:

1. As appropriate, remove the MFI II and Video Controller PCAs first.
2. 2. Detach all connectors (8 to 10 places).
3. 3. Remove the two connector locking posts from the pod connector on the right side of the mainframe.
4. 4. Remove the five corner-retaining screws.
5. Gently work the Main PCA free of its mainframe retaining clips.

SCREEN OVERLAY 4-29.

Recommended Use 4-30.

The Contrast Enhancement Overlay enhances contrast and reduces reflection from external sources.

Removing the Overlay 4-31.

To remove the overlay, spread the fingers of one hand and place your hand on the screen. Close your hand slightly, allowing the friction of your fingers to pull the overlay away from the screen.

Installing the Overlay 4-32.

Use the following procedure to install the Contrast Enhancement Overlay:

1. The overlay has adhesive on both tabs on the side opposite the matte surface. Remove the backing from the adhesive.
2. With the matte surface facing out, insert one overlay tab under the center of the lip at the top of the screen.
3. Insert the other overlay tab under the center of the lip at the bottom of the screen. Hold the overlay in place with your hand.
4. Slip the side of the overlay under the lip at the left side of the screen by simultaneously running your finger along the left edge of the overlay, and sliding the overlay under the screen lip.
5. Spread the fingers of your left hand to hold the left side, top, and bottom of the overlay in place. Use your right hand to insert the overlay right edge under the right edge of the screen lip.
6. Center the overlay. Press firmly directly over the tabs of the overlay to activate the adhesive.

MONITOR ACCESS, REMOVAL, INSTALLATION TECHNIQUES 4-33.

The following instructions pertain to the Monochrome Monitor used with the 9100FT Programmer’s Station and Monochrome Video option.

Removing the Monitor Cover 4-34.

1. Disconnect the line cord from the Monitor.
2. Use a Phillips screwdriver to remove the two screws along the bottom front and the single screw at the top rear.
3. Place the Monitor face down on a flat surface. To protect the screen from scratches, the surface must be covered with a soft cloth or pad.
4. Remove the four Phillips screws securing the tilt-base assembly to the Monitor. Rotate the assembly so that the hole found in the plastic foot successively allows access to each screw.
5. Pull the plastic Monitor case up and off.
6. Replace the Monitor case by reversing these steps.

Accessing the Monitor Chassis 4-35.

1. Remove the five Phillips rear panel securing screws. Do not remove the power panel. See Figure 4-4.

2. Place the Monitor screen face down on a flat surface that is protected by a soft cloth or pad.
3. Swing the bottom chassis cover open. The hinge will allow the chassis cover to open to 90 degrees.
4. To close the Monitor chassis, reverse the above procedure.

Removing the Front Bezel 4-36.

1. Remove the monitor cover as described above.
2. Place the monitor chassis on a flat surface, with the front bezel extended over the edge of the work surface.
3. Locate the six front bezel connector holes. The connector holes are located on each side of the metal chassis, where the plastic snaps from the bezel are inserted in the chassis.
4. Insert a flat screwdriver into each of the connector holes, and push in to disengage the front bezel snaps. Maintain an outward force on the bezel to keep the snaps disengaged.
5. Lift the front bezel away from the chassis.
6. To reinstall the front bezel, position the bezel with the bezel snap fingers in line with the connector holes. Press in evenly on the bezel until all of the front bezel fingers snap into place.

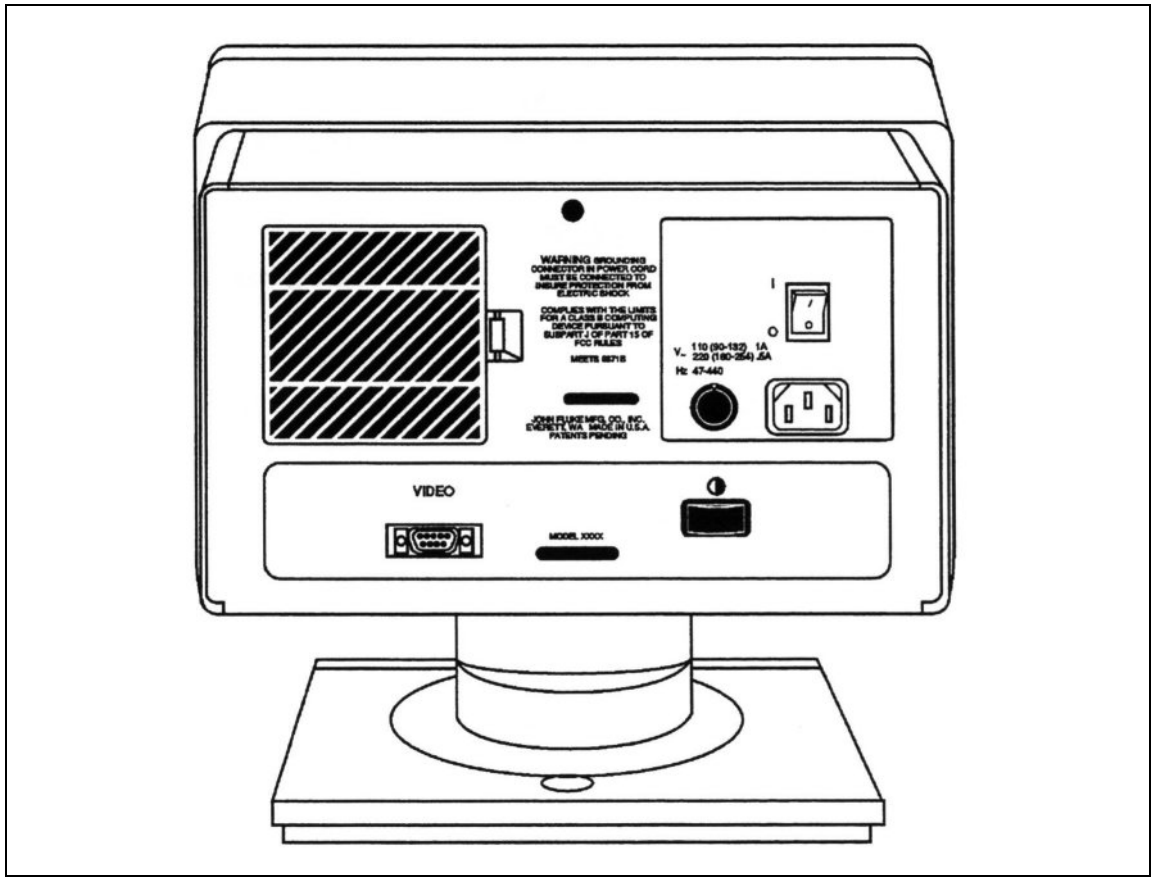


Figure 4-4. Monitor Rear Panel

WARNING

USE EXTREME CAUTION WHEN REMOVING THIS UNIT. THERE IS A DANGER OF ELECTRICAL SHOCK FROM HIGH VOLTAGE STORED IN CAPACITORS.

1. Lethal voltages may be present. Disconnect the power and wait 30 seconds before working with the power supply.
2. Open the chassis as described under the heading, “Accessing the Monitor Chassis”.
3. Place the Monitor face down on a soft, level surface.
4. Disconnect the six wires that connect the power panel to the power supply. Refer to Figure 4-5 for wire locations.
5. Remove the power panel (two Phillips screws).
6. Remove the Phillips screw found in the rear corner of the Power Supply PCA.
7. Now work the Power Supply PCA loose from the three securing standoffs found in the remaining three corners.
8. Holding the Power Supply PCA in one hand, use the other hand to disconnect the power/video cable connector from the power supply. Do not brush against the CRT or yoke.
9. Remove the Power Supply PCA from the chassis.

NOTE

Do not discard the piece of foam that rests between the power supply and the chassis.

The following installation procedure assumes that the existing Power Supply has already been removed:

1. Place the Monitor face down on a soft, level surface.
2. Install three new plastic standoffs into the square holes in the chassis top.

NOTE

Do not reuse plastic standoffs. Damage to standoffs may occur during removal without being clearly apparent. Fluke recommends that PCAs ALWAYS be equipped with new standoffs. All replacement modules are provided with new standoffs.

3. With the power/video cable connector directed toward the rear of the Monitor, connect the power/video cable to the power supply. The power/video cable connector may be fit over any two of the three sets of pins.
4. Reinsert the foam piece between the power supply and the chassis.
5. Place the power supply over the standoffs and press on the PCA to lock it in place. Install the Phillips screw in the rear corner of the pca.
6. Connect the power leads and ground. Refer to Figure 4-5 for wire connections.

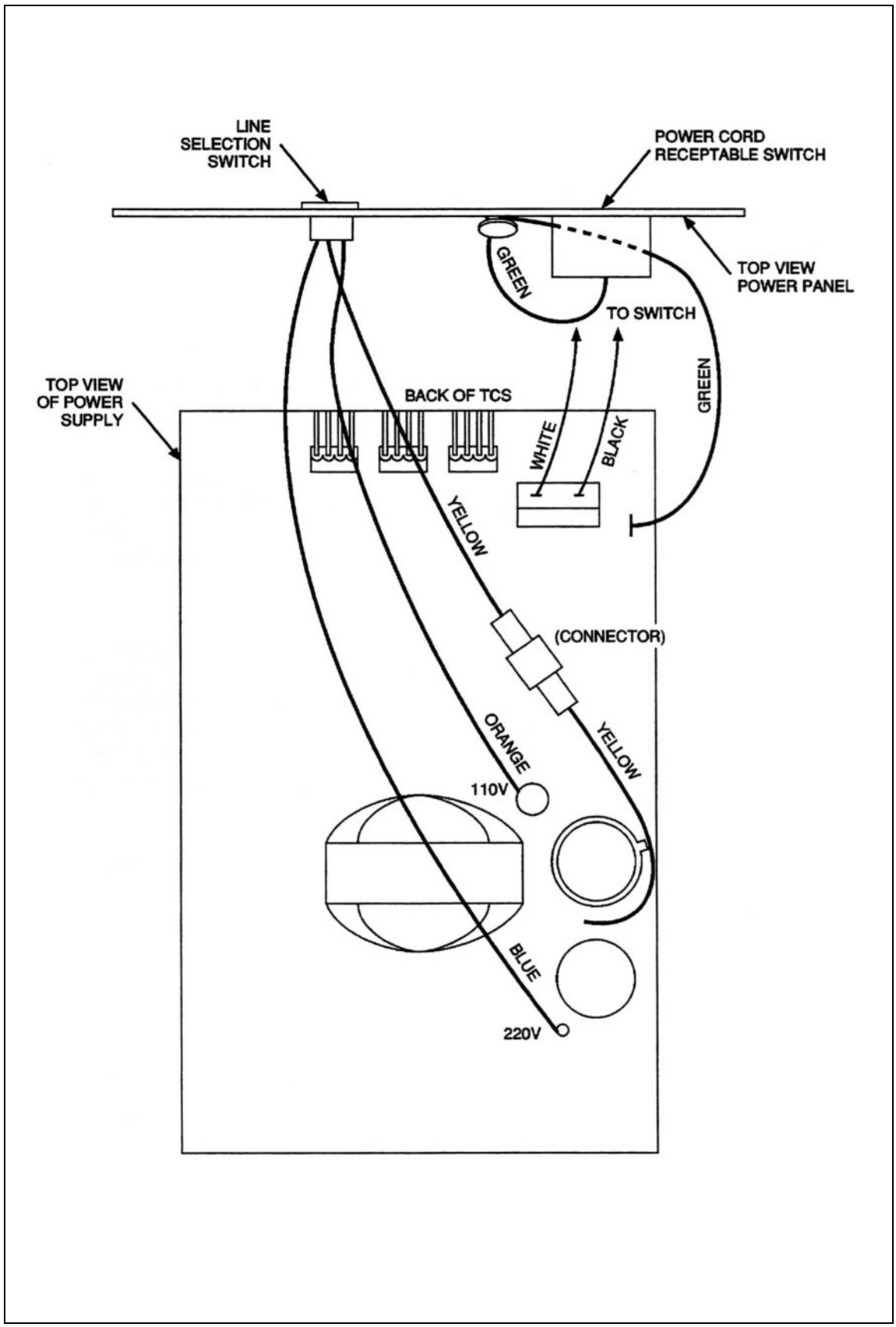


Figure 4-5. Power Supply Lead Connections

NOTE

The mains wiring must not touch the secondary wiring (power/video cable). If wires touch, the unit will probably exceed conducted emissions limits. The power/video cable should be taut against the side of the chassis.

7. Replace the power panel.
8. Close the chassis cover.

NOTE

Fluke recommends replacing the CRT when the Display PCA is replaced.

WARNING

TO REDUCE THE RISK OF ELECTRIC SHOCK ALWAYS TURN OFF THE TCS, DISCONNECT THE POWER CORD FROM THE PANEL ON THE REAR OF THE CHASSIS, AND WAIT ONE MINUTE BEFORE PROCEEDING WITH DISPLAY PCA REMOVAL.

WARNING

THE HIGH VOLTAGE SUPPLY MAY RETAIN A HIGH VOLTAGE CHARGE EVEN AFTER THE INSTRUMENT HAS BEEN TURNED OFF FOR SOME TIME. A CHARGE CAN BUILD UP ON THE CRT ANODE EVEN AFTER IT HAS BEEN DISCHARGED. THE CHARGE CAN DELIVER A SHOCK THAT COULD CAUSE THE CRT TO BE DROPPED, RESULTING IN AN IMPLOSION AND DANGEROUS FLYING GLASS.

1. Open the chassis as described under the heading, “Accessing the Monitor Chassis”.

NOTE

Although the Display PCA uses a bleeder resistor, as a safety precaution assume that the resistor is nonfunctional.

2. Discharge the anode to the CRT through a 1-megohm resistor as follows:
   a. Connect one end of the resistor to the chassis with one clip lead.
   b. Connect the other end of the resistor to the shaft of a 5-inch or longer screwdriver with a 1/4-inch tip, using another clip lead.
   c. Hold the screwdriver by its plastic handle, and gently slip the tip under the edge of the anode connector on the CRT end of the high-voltage lead; keep the blade flat against the glass envelope.
   d. Slide the blade forward until the screwdriver blade touches the metallic clip at the end of the high-voltage lead. Do not scratch the surface of the CRT.

3. Remove the power/video cable connector from the Display PCA. Use both hands to pull the cable vertically away from the Display PCA.

   Do not bend the Display PCA. Refer to Figure 4-6 for the location of the power/video cable.

CAUTION

Bending the Display PCA can break solder joints and result in unreliable operation.

4. Working from the chassis exterior, remove the five standoff-securing screws for the Display PCA.
5. Locate the single black ground wire that attaches to the CRT mounting bracket in the upper corner of the chassis. Pull the ground wire off the tab in the mounting bracket.
6. Gently pull the CRT socket away from the end of the CRT.
7. Disconnect the yoke wire connectors from the Display PCA.
8. Use a side-to-side motion to pry the anode on the CRT loose from the anode connector. If necessary, use a non-conductive tool to help disengage the connector.
9. Remove the four PCA standoffs.
10. Remove the Display PCA with the anode and drive wires attached.

INSTALLING THE DISPLAY PCA 4-42.

NOTE

Fluke recommends replacing the CRT when the Display PCA is replaced.

WARNING

TO REDUCE THE RISK OF ELECTRIC SHOCK ALWAYS TURN OFF THE 9100FT/9105FT, DISCONNECT THE POWER CORD FROM THE PANEL ON THE REAR OF THE CHASSIS, AND WAIT ONE MINUTE BEFORE PROCEEDING WITH DISPLAY PCA INSTALLATION.

1. Open the chassis as described under the heading, “Accessing the Monitor Chassis”.
2. Use a Phillips screwdriver to remove the two screws on the power panel. Disconnect the six wires that connect the power panel to the power supply. Refer to Figure 4-5 for wire locations. Remove the power panel.
3. Install the Display PCA using four standoffs. Do not bend the Display PCA.

CAUTION

Do not bend the Display PCA. Doing so can break the solder joints and result in unreliable operation.

4. Replace the power/video cable connector in the Display PCA.
5. Snap the anode connector to the top of the CRT.

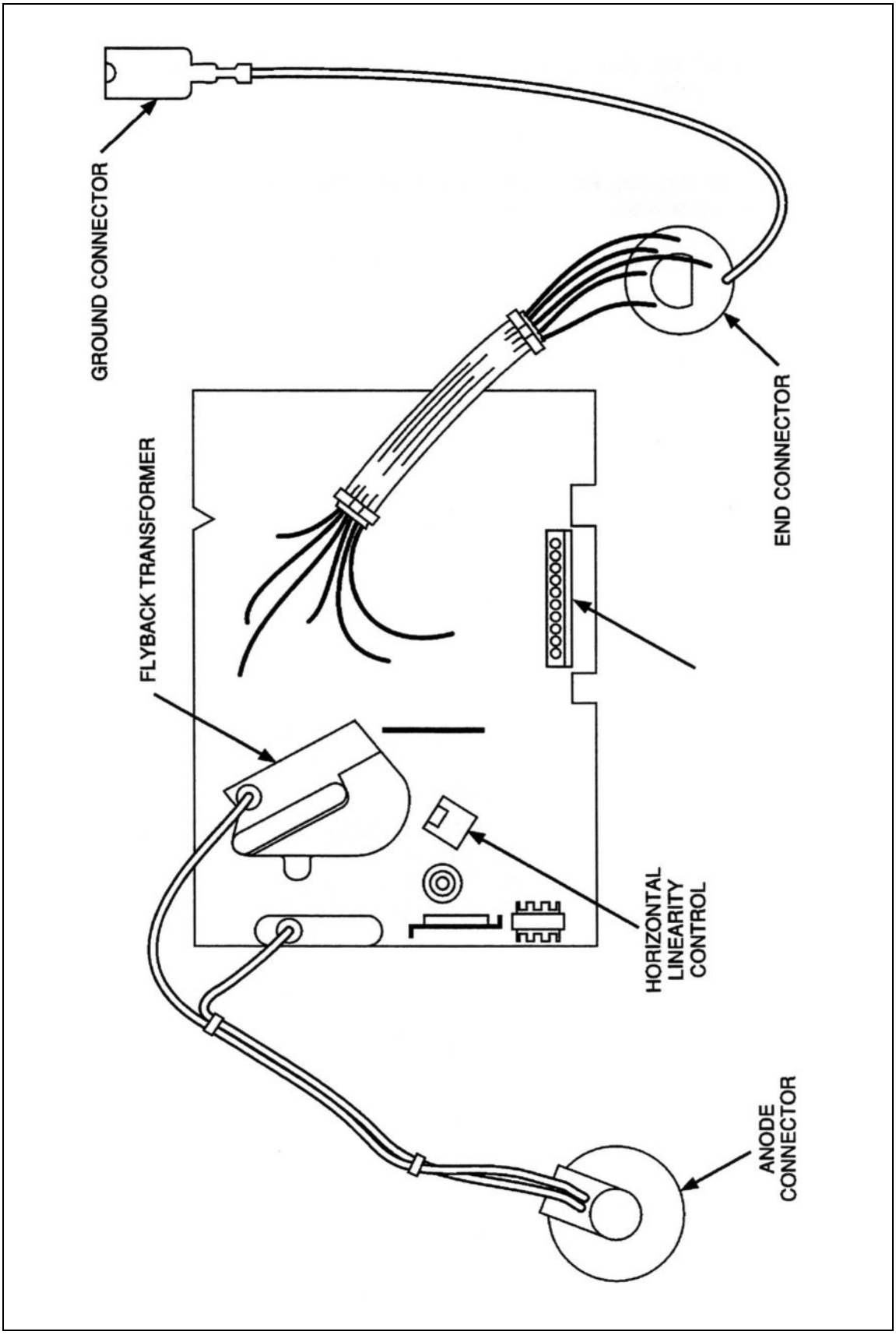


Figure 4-6. Display PCA

6. Reattach the CRT neck connector to the top of the neck of the CRT. The connector is keyed to the pins.
7. Reconnect the yoke connectors.
8. Reattach the black ground wire to the tab on the CRT mounting bracket beneath the X-ray warning on the chassis.
9. Reconnect the six wires that connect the power panel to the power supply. Refer to Figure 4-5 for wire locations. Replace the power panel.
10. Close the chassis cover as described under the heading, “Accessing the Monitor Chassis”.

NOTE

Fluke recommends replacing the Display PCA when the CRT is replaced.

WARNING

TO AVOID INJURY, USE CAUTION WHEN HANDLING THE CRT. WEAR PROTECTIVE CLOTHING AND SAFETY GLASSES OR A FULL FACE SHIELD. AVOID STRIKING THE CRT ON ANY OBJECT THAT MIGHT CAUSE IT TO CRACK OR IMPLODE. NEVER HANDLE THE CRT IN AN UNSAFE AREA, SUCH AS ONE WITH WET FLOORS OR HIGH ACTIVITY. NEVER HANDLE THE CRT AROUND OTHERS WHO MAY NOT BE PROPERLY PRO- TECTED. AVOID SCRATCHING THE TUBE OR CAUSING OTHER DAMAGE DURING INSTALLATION.

WARNING

TO REDUCE THE RISK OF ELECTRIC SHOCK ALWAYS TURN OFF THE 9100FT/9105FT, DISCONNECT THE POWER CORD FROM THE PANEL ON THE REAR OF THE CHASSIS, AND WAIT ONE MINUTE BEFORE PROCEEDING WITH CRT AND YOKE REMOVAL.

WARNING

THE HIGH VOLTAGE SUPPLY MAY RETAIN A HIGH VOLTAGE CHARGE EVEN AFTER THE INSTRUMENT HAS BEEN TURNED OFF FOR SOME TIME. A CHARGE CAN BUILD UP ON THE CRT ANODE EVEN AFTER BEING DISCHARGED. THE CHARGE CAN DELIVER A SHOCK THAT COULD CAUSE THE CRT TO BE DROPPED, RESULTING IN AN IMPLOSION AND DANGEROUS FLYING GLASS.

1. Discharge the anode to the CRT through a 1-megohm resistor as follows:
   a. Connect a resistor end to the chassis with clip lead.
   b. Connect the other end of the resistor to the shaft of a 5-inch or longer screwdriver with a 1/4-inch tip, using another clip lead.

c. Hold the screwdriver by its plastic handle, and gently slip the tip under the edge of the anode connector on the CRT end of the high-voltage lead; keep the blade flat against the glass envelope. Slide the blade forward until the screwdriver blade touches the metallic clip at the end of the high-voltage lead. Do not scratch the surface of the CRT.

2. Disconnect and remove the Display PCA as follows:
   a. Gently pull the CRT socket away from the end of the CRT.
   b. Disconnect the yoke wire connectors from the Display PCA.
   c. Use a side-to-side motion to pry the anode on the CRT loose from the anode connector. If necessary, use a non-conductive tool to help disengage the connector.
   d. Remove the four pca standoffs.
   e. Remove the Display PCA with the anode and drive wires attached.
3. Use a Phillips screwdriver to remove the two screws on the power panel.
4. Disconnect the six wires that connect the power panel to the power supply. Refer to Figure 4-5 for wire locations. Lift off the power panel.
5. Remove the front bezel (see “Removing the Front Bezel”, earlier in this section.)
6. Use a Phillips screwdriver to remove the eight outside screws from the four CRT mounting brackets. Remove the tab from the CRT mounting bracket at the corner of the CRT.
7. Remove the dust gasket.
8. With the CRT face down (on a soft, level surface), lift the chassis off the CRT. Do not scratch any part of the CRT!
9. Place the CRT on a soft, level surface.

INSTALLING THE CRT AND YOKE 4-45.

NOTE

Fluke recommends replacing the Display PCA when the CRT is replaced.

WARNING

TO AVOID INJURY, USE CAUTION WHEN HANDLING THE CRT. WEAR PROTECTIVE CLOTHING AND SAFETY GLASSES OR A FULL FACE SHIELD. AVOID STRIKING THE CRT ON ANY OBJECT THAT MIGHT CAUSE IT TO CRACK OR IMPLODE. NEVER HANDLE THE CRT IN AN UNSAFE AREA, SUCH AS ONE WITH WET FLOORS, HIGH ACTIVITY, ETC. NEVER HANDLE THE CRT AROUND OTHERS WHO MAY NOT BE PROPERLY PROTECTED. AVOID SCRATCHING THE TUBE OR CAUSING OTHER DAMAGE DURING INSTALLATION.

WARNING

TO REDUCE THE RISK OF ELECTRIC SHOCK ALWAYS TURN OFF THE 9100FT/9105FT, DISCONNECT THE POWER CORD FROM THE PANEL ON THE REAR OF THE CHASSIS, AND WAIT ONE MINUTE BEFORE PROCEEDING WITH CRT AND YOKE INSTALLATION.

WARNING

THE HIGH VOLTAGE SUPPLY MAY RETAIN A HIGH VOLTAGE CHARGE EVEN AFTER THE INSTRUMENT HAS BEEN TURNED OFF FOR SOME TIME. THE CHARGE CAN DELIVER A SHOCK THAT COULD CAUSE THE CRT TO BE DROPPED, RESULTING IN AN IMPLOSION AND DANGEROUS FLYING GLASS.

The Display PCA and power panel must be removed prior to CRT installation.

1. With the CRT face down on a soft, level surface and the anode facing away from you, loosely install the four CRT brackets to the four CRT mounting ears and CRT grounding clip (step 2).

CAUTION

Do not move the magnets on the CRT yoke.

2. Insert the CRT grounding clip under the screw on your right, closest to you. Insert the ground wire tab into the clip.
3. Carefully insert the chassis over the CRT with the anode connection on the CRT positioned toward the top of the unit.
4. Use a Phillips screwdriver to install and loosely tighten the eight exterior screws on the four CRT mounting brackets.
5. Approximately center the CRT. Use a long-bladed screwdriver to tighten the four screws that attach the CRT to the CRT mounting bracket.
6. Push the CRT as far forward as possible into the chassis and tighten the exterior screws.
7. Clean the CRT with alcohol or another suitable cleaner.
8. Reinstall the Display PCA as described above.
9. Reinstall the dust gasket.
10. Reinstall the front bezel.
11. Reconnect the six wires that connect the power panel to the power supply. Refer to Figure 4-5 for wire locations. Reinstall the power panel by replacing the two screws.
12. Perform the procedure under the heading “Monitor Adjustment.”
13. Close the chassis cover.

MONITOR ADJUSTMENT 4-46.

NOTE

Display tilt may be slightly affected by the orientation of the Monitor, especially in environments containing a high density of metal. Rotate the unit and try to find a position where the tilt is in the center between extreme clockwise tilt and extreme counterclockwise tilt. Perform alignment and adjustment in that position. If no difference is perceived between the two extremes, proceed in the most convenient orientation.

NOTE

Magnetic alignment is accomplished with alignment magnets. Magnets should not be removed or added to the CRT yoke. The displays are prealigned. Due to handling, however, a magnet may be rotated off position. Rotate the magnets to improve alignment ONLY IF ABSOLUTELY NECESSARY. It should not be necessary to use the centering rings on the yoke to align the display.

CAUTION

Turning the Monitor on with line voltage higher than 132V ac when the line voltage selection switch is in the 110 position will damage the power supply. If the voltage is set for 180 to 264V and 90 to 132V is applied, the unit may not operate.

NOTE

Allow the Monitor to warm up for at least 10 minutes. During the first 5 minutes of operation, raster lines may be visible on the display. This is common to CRT displays and is not a fault.

The display can be adjusted using a program-generated monitor alignment pattern. The pattern consists of four outlined boxes, two across and two down. Each box is 40 characters wide by 12 lines high. This program is used with the Alignment Template, P/N 777144. When the display is properly adjusted, the four boxes displayed by the program fit evenly and symmetrically within the inner lines of the template.

Use the following monitor alignment program. An alignment pattern can also be generated by a program on the 9100 Series Utility Disk, which is part of the 9100FT Service Kit (see Troubleshooting).

```
$************************************************************************
!*  This program generates an alignment pattern on the monitor. The         *
!*  pattern consists of four outlined boxes, two across and two down;       *
!*  each box is 40 characters wide and 12 lines high.                       *
$************************************************************************

HL9 = "8A"+"\8A"+"\8A"+"\8A"+"\8A"+"\8A"+"\8A"+"\8A"+"\8A" ! 9 horiz. lines
Top_s ="\86"+"\8A"+ HL9 + HL9 + HL9 + HL9 +"\8A"+"\8C"  ! top of box string
Bot_s ="\83"+"\8A"+ HL9 + HL9 + HL9 + HL9 +"\8A"+"\89" ! bottom of box string
Ctr_s ="\85                                        \85" ! middle (88 spaces)
EoS_s ="\1B[2;30H Monitor \1B[4C Alignment \1B[10B"  ! End of Screen string
L12_s =""                                        ! Line 12 string

open device "/term2", as "output"      ! open channel to print to monitor

print using "\1B[H\1B[J"        ! cursor to top left, and clear monitor screen

loop for s = 0 to 1             ! do top half and then bottom half of pattern
  print Top_s,Top_s             ! print top line of left and right boxes
  loop for 1 = 2 to 11
    print Ctr_s,Ctr_s           ! fill in center of left and right boxes
  end loop
  if s > 0 then L12_s = EoS_s   ! if this is the End of the Screen, then
                                !   need to print title and position cursor.
  print Bot_s,Bot_s,L12_s       ! print bottom line of left and right boxes

end loop                        ! if this was the top half, do the bottom

end program
```

Alternatively, any monitor display pattern can be used when the programmed pattern is not available. This method involves display and adjustment of the monitor screen for a centered display of the correct size. The alternative pattern used must measure 80 columns wide by 24 rows high to allow for correct adjustment.

The monitor display is adjusted using the following seven controls:

- Vertical Linearity
- Vertical Size
- Brightness
- Focus
- Horizontal Phase
- Horizontal Size
- Horizontal Linearity
- Contrast

The first six of these controls can be adjusted externally through holes in the monitor chassis (shown in Figure 4-7). Adjusting horizontal size requires hex adjustment tool (P/N 572321). Contrast is an external operator adjustment. Adjusting all other controls requires the use of an adjustment tool (P/N 800540).

The monitor chassis must be opened to adjust the Horizontal Linearity control. Refer to "Accessing the Monitor Chassis". Adjusting the Horizontal Linearity control requires the use of the hex adjustment tool (P/N 572321).

As some adjustments may interact with others, repeating the procedure may be necessary. For either display method, use the following steps to adjust the display:

1. If necessary, remove the monitor cover. Then, locate the external display adjustment holes. See Figure 4-7.
2. Cover a flat surface with a soft cloth to protect the monitor screen. Place the Monitor face down.
3. Open the Monitor by using a Phillips screwdriver to remove the five screws on the rear panel. Swing the bottom chassis cover down. Do not remove the power panel.
4. Perform the following yoke adjustment only if the screen appears tilted.
   a. Loosen the clamp around the yoke of the CRT using a 3/16-inch nut driver.
   b. Turn the Monitor so that the display can be seen.
   c. Rotate the yoke slightly to adjust for the screen tilt.
   d. Check that the tightening screw is easily accessible, then tighten the clamp to a torque of 6 inch-pounds (0.678 n-m). Do not overtighten the screw, or the neck of the CRT may crack.

WARNING

TO AVOID INJURY, USE CAUTION WHEN HANDLING THE CRT. WEAR PROTECTIVE CLOTHING AND SAFETY GLASSES OR A FULL FACE SHIELD. AVOID STRIKING THE CRT ON ANY OBJECT THAT MIGHT CAUSE IT TO CRACK OR IMPLODE. NEVER HANDLE THE CRT IN AN UNSAFE AREA, SUCH AS ONE WITH WET FLOORS, HIGH ACTIVITY, ETC. NEVER HANDLE THE CRT AROUND OTHERS WHO MAY NOT BE PROPERLY PROTECTED. AVOID SCRATCHING THE TUBE OR CAUSING OTHER DAMAGE DURING INSTALLATION.

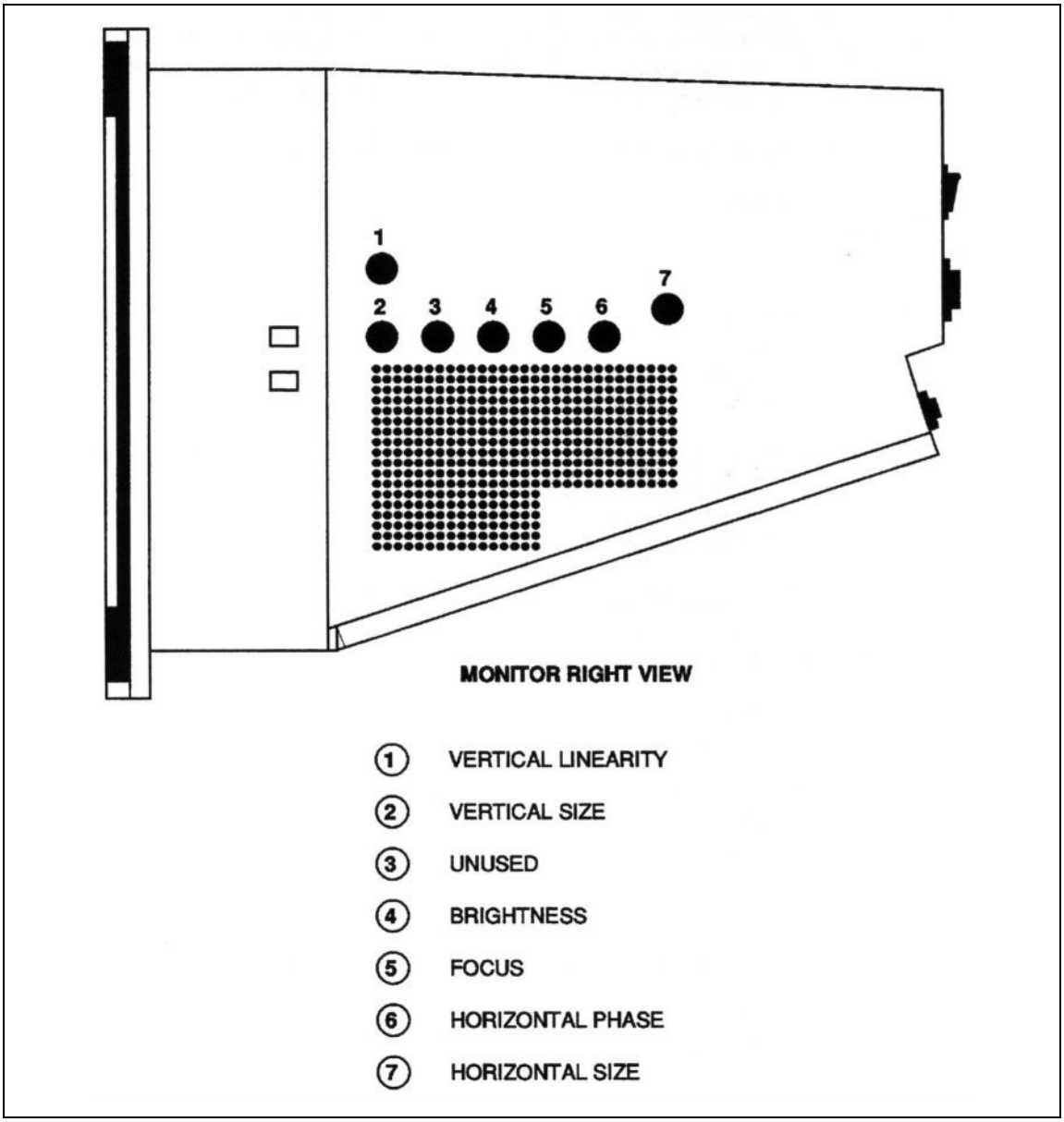


Figure 4-7. External Display Adjustment Locations

NOTE

Display tilt may be slightly affected by the orientation of the Monitor, especially in environments containing a high density of metal. Rotate the unit and try to find a position where the tilt is in the center between extreme clockwise tilt and extreme counterclockwise tilt. Perform alignment in that position. If no difference is perceived between the two extremes, proceed in the most convenient orientation.

5. Locate the Horizontal Linearity control on the Display PCA (see Figure 4-7.) Adjust Horizontal Linearity so that the left half of the display is the same size as the right half of the display. Since the open chassis cover has a slight effect on Horizontal Linearity, close the chassis cover to verify Horizontal Linearity and keep it closed

for the remainder of the procedure. Linearity is also slightly affected by the unit being upside down.

6. Adjust Horizontal Phase to line up the center gaps between the boxes with the alignment centering marks on the bezel. If an alternative pattern is being used, use Horizontal Phase to center the display.
7. Adjust Vertical Linearity so that the boxes (or regions of the alternative pattern) appear the same.
8. Adjust Vertical Size to make the alignment pattern (or alternative pattern) about 5 1/8 inches (130 mm) high.
9. Adjust Horizontal Size to make the alignment pattern (or alternative pattern) about by 7 3/4 inches (195 mm) wide.
10. Set the Brightness control for a slight amount of “blooming” with the Contrast (external operator control) set to maximum.
11. Adjust the Focus control with Contrast set for normal viewing.
12. Use a Phillips screwdriver to replace the five rear panel screws.

NOTE

If the Monitor was adjusted with the unit upside down, a final Horizontal Phase adjustment will probably be necessary,

13. Reinstall the monitor cover.

DECIDING ON CRT REPLACEMENT 4-47.

The CRT should be replaced if any of the following occur:

- If an image has been burned into the phosphor and the image on the display is unacceptably altered.
- If scratches are detectable by a pass of the finger. (Scratches can create a safety hazard that lessens the ability of the CRT to withstand implosion.)

The CRT may require replacement when any of the following occur:

- Ghost images appear on the display.
- Brightness levels are unacceptable.

NOTE

Insufficient brightness can be caused by several factors. After 10,000 hours of continuous excitation of the phosphor, CRT brightness can be expected to have dropped by approximately 50 percent. Failures in the Display PCA can also cause loss of brightness.

A properly functioning CRT requires ten minutes to warm up completely. During the first five minutes, raster lines may appear on the display. This is common to CRT displays and is not a fault. If the display takes more than five minutes to achieve full brightness, suspect either a CRT or Display PCA failure.

NOTE

Monitors are preset at the factory for the same brightness at maximum contrast. Due to CRT variations, the Display PCA brightness control will not be in the same position for all units and the raster may be visible for varying amounts of time, if at all.

NOTE

Because the maximum brightness of the CRT will vary from unit to unit, the decision to replace a display on the basis of insufficient brightness is subjective.

SELF TEST ROUTINES 4-47.

Power-Up Self Test 4-48.

At power-up, the 9100FT/9105FT sequences through a series of self tests. A display response is presented for any test that fails. These responses (and related meanings) are presented in Table 4-2. In addition, a Display ROM and Display Response test is run. A failed test in this instance is evidenced by simultaneously flashing RUN UUT and DISK ACCESS LEDs.

Probe Self Test 4-49.

The Probe Self Test verifies that the Probe is connected and is communicating with the system. Use the following procedure:

1. Press the MAIN MENU key.
2. Press the left arrow (<--) key until the cursor rests on the first (left-most) field. Then, with the cursor on this field, press the SELFTEST key.
3. Press the right arrow (-->) key to move the cursor to select the next field, then press the PROBE key. Check that the display reads:

   MAIN: SELFTEST PROBE
4. Press the ENTER key to initiate the self test.
   - If the self test fails, a failure message is displayed. Check the probe connection and repeat the test.
   - If the test fails a second time, the Probe requires service.

Pod Self Test 4-51.

This test performs a comprehensive pod check. Test failure is evidenced by an error message. (See the respective pod manual for full error descriptions). Proceed as follows:

1. Make all connections. Ensure that the Pod is attached to the mainframe and that the pod UUT connector is inserted and locked into the pod self-test socket. The pod manual and the 9100FT/9105FT Getting Started guide illustrate these connections further.
2. On the 9100FT/9105FT, first press MAIN MENU, then move the cursor to the first (left-most) field using the left arrow (<--) key.
3. Press the SELFTEST key.
4. Move the cursor one field to the right and press POD. Check that the display reads: MAIN: SELFTEST POD
5. Press ENTER to initiate the self test.
   - If the self test fails, a failure message is displayed. Check the pod connection and repeat the test.
   - If the test fails a second time, the Pod requires service.

I/O Module Self Test 4-52.

The I/O Module Self Test verifies that the I/O Module is connected and is communicating with the system. Use the following procedure:

Table 4-2. Power-Up Self Test Responses

selftest:	Explanation
testing memory...	This message is displayed during the simple read/write test of the RAM.
---Press any key to continue test--- or the RESET key for the next test If an error was detected during the RAM test, pressing the RESET key aborts the RAM test and sequences the 9100FT/9105FT to the next test in the power-up self test series. Pressing any other key continues the test at the next higher RAM location.	
ram read/write error @	A RAM read/write test has failed at the specified address. The memory test itself is extremely primitive. A long word with a value of '5a5a5a5a' is written and read back, followed by a long word with the value 'a5a5a5a5'. Any bit that cannot be written either high or low is considered defective.
r/w error on pod cmd port:	Of the command bits that are tested on the pod port, one or more have failed a read/write test. The mask of the failing bit(s) is displayed in hex.
r/w error on pod data port:	One or more bits in the pod data port have failed a read/write test. An error mask of the failing bit(s) is displayed in hex.
data error in uart u7 should be: xxxx not: xxxx	An error occurred while the UART was inits digital loopback self-test mode. The data written has not matched the data read in device U7, and the two datum are displayed on the second line of the display.
data error in uart u12 should be: xxxx not: xxxx	An error occurred while the UART was in its digital loopback self-test mode. The data written has not matched the data read in device U12, and the two datum are displayed on the second line of the display.
timed out waiting for uart	One of the UART transmit registers has not cleared in a reasonable amount of time. The UART clock could be disabled, or the chip itself could be bad.
probe i/o board not responding	A simple read/write test to both of the gate array chips on the Probe I/O-ECL PCA has failed.
ram test bus error@	An unexpected bus error occurred during the power up RAM test. This could be a result of setting the RAM size in the EEPROM too large, or it could be a problem with the memory decoding circuitry.
front display not responding	The front panel display processor has not returned the expected character within a reasonable amount of time.
probe i/o stop counter failure	The high speed stop counter in the start-stop logic has failed. To test the stop counter on the Probe I/O-ECL PCA the counter is soft clocked and checked for proper response. The counter is preset to a value of two. The clock is soft stepped once and the stop counter is checked to insure it has not triggered. Another clock is produced and the stop counter is checked for an active condition.
probe i/o logic chip inactive	In the process of setting up the stop counter test, it is necessary to set the start-stop state machine inside the U19 gate array to state 1 (start received, waiting for stop). If the state machine is not in state 1 after clocking, an error is assumed somewhere in the start-stop logic subsection.
floppy controller failure	A simple read/write test to several of the floppy controller registers has failed.
floppy controller not responding	A bus error occurred while trying to read or write the floppy controller.

Table 4-2. Power-Up Self Test Responses (cont)

selftest:	Explanation
stuck vector:	The floppy controller is given a force interrupt command. If the resultant vector is not the floppy controller interrupt vector, then it is assumed that another interrupt is active. At this point in the self test, no interrupts should be active, and this is considered an error. The force interrupt command is followed by a reset interrupt command. After this command no interrupts should be active, and any active interrupts are again considered error conditions. In both conditions the number reported is the actual physical vector address.
uarts not responding	A bus error occurred while trying to read or write either of the UART devices.
front display ram test failure	An error code was returned by the front panel display when asked to perform an internal RAM test.

1. Press MAIN MENU, then move the cursor to the first (left-most) field using the left arrow (<--) key.
2. Press SELFTEST.
3. Move the cursor one field to the right and press I/O MOD.
4. Move the cursor one more field to the right, and press the number of the I/O Module to be tested. Check that the display reads:

   MAIN: SELFTEST I/O MOD <n>

   (where <n> signifies the number of the I/O Module)
5. Press ENTER to initiate the self test.
   - If the self test fails, a failure message is displayed. Check the I/O Module connection and repeat the test.
   - If the test fails a second time, the I/O Module requires service. (If the failure message displays a failing pin mask, the MSB or left most bit of the mask represents I/O pin 40, and the LSB represents pin 1.)

Display Self Test 4-53.

Several software tests aid in testing the Display Interface PCA. Each test can be selected by a command sent through the display processor serial port. The “Test” command, 0x0e, followed by a test number ascii 1-9 (or 0x31-0x39) selects the test.

The tests are available through a program in the 9100FT Service Kit. These tests are not available through TL/1 programs; the Control N (0x0e) command is not sent to the display.

Tests 1 (ROM) and 2 (RAM) are also performed by mainframe software during the mainframe self test following a reset. At this time, the mainframe also performs Test 9 (look for Synchronous Special Function key) to determine if a boot should be forced off the floppy drive instead of the hard disk.

Tests 4, 5, and 6 are useful for troubleshooting the keyscan and display refresh hardware. They are available by grounding Test Point 6 (TP6) on the Display Interface PCA during a reset, as well as by software control.

All display tests are listed and described in Table 4-3.

PERFORMANCE TEST 4-54.

Tests Using the Service Utility Disk 4-55.

Insert the Service Utility disk into the floppy disk drive (top drive on 9105FT.) Connect the mainframe to line power and power up the 9100FT/9105FT. Press and hold the three keys: SOFT KEYS, F2, and F4. Then run the following self tests:

Table 4-3. Display Self Test

TEST	DESCRIPTION
0	Sends Out Software Revision Number The number is returned to the serial port just like a key press.
1	Verifies ROM Internal Checksum Returns 0x70 (p) to the serial port if test passed, 0x71 (q) if it didn't.
2	Performs Quick RAM Test This is a non-destructive test of the Display RAM. It writes the complement of the present data, reads it back, rewrites the original data, and then reads that back. Returns Ox72 (r) to the serial port if the test passed, 0x73 (s) if it didn't.
3	Performs Long RAM Test This is a more complete, destructive test of the Display RAM. It performs a test similar to the 9100 RAM FAST on the RAM and returns 0x74 (t) to the serial port if the test passed, or 0x75 (u) if the test did not pass.
NOTE Tests 4, 5, and 6 cause the software to exit mainframe control. The Display Board does not respond to further commands or data until the test is exited by keyboard control or by a reset. All three tests are destructive, in that they write over the present display. Tests 4, 5, and 6 can be accessed by grounding the TEST testpoint (TP6 on the Display Interface PCA) and resetting (or powering on) the display.	
4	Jump to Key Test Routine This is the mode entered when TP6 is grounded during a reset. This test displays the row and column of the key being pressed on the display. The RESET key causes this test to terminate and Test 5 to start.
5	Jump to Display Lines Routine The following key-pattern relationships are applicable during this test: Keys 1, 2, and 3 each display a vertical bar in every third column. For example, key 1 displays bars in columns 1, 4, 7, and so on. Keys 2 and 3 control columns beginning at 2 and 3, respectively. Keys 4, 5, and 6 display a series of horizontal bars, also spaced three lines apart. Key 0 turns all lines off (blank display). Key 7 turns all lines on and is the default when test 5 is entered.
NOTE This mode is useful if the display has a "burned in" problem. Since this mode does not time out, leaving the display in this mode overnight makes for a more even display.	

Table 4-3. Display Self Test (cont)

TEST	DESCRIPTION
	The EXEC Key returns to Test 4. The ALPHA Key jumps to Test 6. The RESET Key exits these tests entirely and returns the display to mainframe control.
6	Jump to V-H Lines Routine This routine identifies the bad grid drivers or row drivers. The arrow keys are used to move the displayed cross hairs. Pressing the HELP key displays the names of the two grids and one row driver which should be on to illuminate the dot at the intersection of the cross hairs. Pressing the RESET Key returns to Test 5.
7	Unlock Keyboard If the keyboard has been locked by test 8, this command re-enables the key scan. It returns 0x76 (v) as an acknowledge byte.
8	Lock Keyboard This command disables key scan and prevents the display board from sending any key press information. It is used by the mainframe to ensure that only test routine data is received. It returns 0x77 (w) as an acknowledge byte.
9	Report Synchronous Special Function Key This function returns a 0x79 (y) if the processor has seen the special function key press since the last inquiry or reset. It returns a 0x78 (x) if it has not seen it. The Special function results from the SOFT KEYS, F2, and F4 keys being pressed simultaneously.

1. Run the DISPLAY TEST utility program.

2. Perform the following display tests: RAM TEST, ROM TEST, SELF TEST.

3. Now press any key, then RESET to run the V-H lines self test. Check the display patterns accessed with keys 0 through 7, as follows:

KEY	DISPLAY PATTERN
0	Display off
1	Vertical line pattern
2	Vertical line pattern
3	Vertical line pattern
4	Horizontal line pattern
5	Horizontal line pattern
6	Horizontal line pattern
7	All pixels on

4. Press the EXEC key to run the Keypad self test. Press each of the keypad keys and check the column/row numbers displayed.

5. Press RESET twice, and then EXIT.

Now run VIDEO ALIGN PATT (if the Video Controller is installed and a monitor is available). Run PRG KEYBD TEST (if a Programmer's keyboard is available).

Self Tests 4-56.

Make the following self-test preparations:

1. Turn off power to the 9100FT/9105FT.
2. Connect a Probe, a Clock Module, I/O Modules (1, 2, 3, or all 4), and an Interface Pod; plug the interface pod UUT or adapter cable into the self-test connector.
3. Power up the 9100FT/9105FT normally (an 'enabled line causes timeout' fault is typical for most interface pods). When READY is returned, proceed with the following tests.

Self test the pod by pressing MAIN MENU, selecting SELFTEST POD, and pressing ENTER YES.

Self test the probe by pressing MAIN MENU and right arrow, selecting SELFTEST PROBE, and pressing ENTER YES.

Self test all four I/O Module positions with the following procedure:

1. Press MAIN MENU. To self test the I/O Module 1 (the first I/O Module connector), press SELFTEST I/O MOD 1 and ENTER YES.
2. Next, if no I/O Module is installed in the second I/O Module connector, move the I/O Module to that second connector. Press MAIN MENU, SELFTEST I/O MOD 2, and ENTER YES to self test I/O Module 2.

NOTE

Either an 'I/O module overcurrent fault' or a 'CAN'T TRISTATE ALL PINS ON I/O MOD' fault may occur if the I/O Module was connected after power up. If this happens, self test the I/O Module again.

3. If necessary, move the I/O Module to the third connector. Press MAIN MENU, SELFTEST I/O MOD 3, and ENTER YES to self test I/O Module 3.
4. If necessary, move the I/O Module to the fourth connector. Press MAIN MENU, SELFTEST I/O MOD 4, and ENTER YES to test I/O Module 4.

Probe Tests 4-57.

COMPENSATE THE PROBE 4-58.

Use the following steps to run the probe compensation:

1. Press MAIN MENU twice, select CAL PROBE COMP, and press ENTER YES.
2. Connect the probe to TRIGGER OUTPUT on the rear panel.
3. Connect an oscilloscope using a compensated 10-to-1 probe to the CAL OUT and COMMON test points accessible through holes on the right side panel.
4. Adjust COMP ADJ for a good square wave with 10% overshoot.
5. When finished, press the STOP key and disconnect the oscilloscope.

CALIBRATE PROBE TO EXT 4-59.

Use the following procedure to calibrate the Probe to EXT:

1. Press MAIN MENU, CAL PROBE TO EXT, and ENTER YES.

2. Connect the CLOCK line (yellow wire) of the Clock Module to the probe tip and the COMMON line (black wire) to the probe ground clip.

3. Press the probe ready button.

CONNECT THE INTERFACE POD 4-60.

Connect the interface pod to a working Unit Under Test (UUT). If a working UUT is not available, the standard interface pod can be used as a dummy UUT; use the following procedure:

1. Connect the pod UUT cable to the selftest socket.

2. From the SETUP MENU on the 9100FT or 9105FT, make the following selection:

   SETUP POD REPORT FORCING SIGNAL ACTIVE OFF

3. Then, for each forcing signal name, select:

   SETUP POD ENABLE xxx OFF

A Memory Interface pod cannot be used as a dummy UUT.

CHECK PROBE DATA SYNC 4-61.

Use the following procedure to check the probe data sync:

1. Press SYNC and set SYNC PROBE TO POD DATA.

2. Press READ, select READ FAST FOREVER ADDR 0, and press ENTER YES.

3. Check the TRIGGER OUTPUT with an oscilloscope for a low-going TTL level pulse.

4. Press STOP to exit this test.

CHECK PROBE EXT SYNC 4-62.

Use the following procedure to check the probe EXT sync:

1. Select SYNC PROBE TO EXT ENABLE ALWAYS CLOCK, up arrow, START, down arrow, STOP COUNT 256 and press ENTER YES.

2. Press PROBE, select OUTPUT PROBE PULSER HIGH, and press ENTER YES.

3. Connect the Clock Module's CLOCK (yellow) and START (green) lines to a TTL signal source with an output frequency between 1 kHz and 40 MHz; connect the COMMON line to the signal source common.

4. To check probe EXT sync operation, press PROBE twice, select ARM PROBE FOR CAPTURE USING SYNC, and press ENTER YES. Then press PROBE, select SHOW CAPTURED RESPONSES, and press ENTER YES. The displayed responses should be:

```
SIG= BB34     ASYNC LEVEL= 1X
COUNT= 1      CLOCKED LEVEL= 1
```

5. To exit this test, press PROBE, set OUTPUT PROBE PULSER OFF, and press ENTER YES.

CHECK PROBE FREQUENCY 4-63.

1. Connect the probe tip to an accurate TTL frequency source.

2. Connect the probe ground lead to the source common.
3. Press PROBE twice, then press SOFT KEYS
4. Select FREQ AT PROBE, and press ENTER YES. Check that the frequency reading is within specification (250 ppm +- 20 Hz).

CHECK PROBE THRESHOLDS 4-64.

Use the following procedure to check the probe thresholds:

1. Press SYNC and select SYNC PROBE TO FREERUN CLOCK. Press PROBE, and select SET PROBE LOGIC LEVEL TO TTL.
2. Connect the probe ground lead to the common of a variable DC power supply. Connect a voltmeter across the output of the power supply and make the following checks:
   - Apply +0.6V to the probe tip. Check that the green light on the probe is on and that the yellow and red lights are off.
   - Apply +1.0V, then +2.2V. Check that only the yellow light is on.
   - Apply +2.6V. Check that only the red light is on.
3. Press PROBE, select SET PROBE LOGIC LEVEL TO CMOS, and make the following checks:
   - Apply +0.8V to the probe tip, and check that only the green light is on.
   - Apply +1.2V, then +3.3V. Check that only the yellow light is on.
   - Apply +3.7V. Check that only the red light is on.
4. Press PROBE, set SET PROBE LOGIC LEVEL TO RS232, and make the following checks:
   - Apply -3.2V to the probe tip. Check that only the green light is on (move the probe ground lead if necessary to apply the negative voltage).
   - Apply -2.8V, then +2.8V. Check that only the yellow light is on (move probe ground lead again if necessary to apply the positive voltage).
   - Apply +3.2V. Check that only the red light is on.
5. Press PROBE, set PROBE LOGIC LEVEL to ECL, and make the following checks:
   - Apply -1.6V to the probe tip. Check that only the green light is on. If necessary, move the probe ground lead to apply the negative voltage.
   - Apply -1.4V. Check that only the yellow light is on.
   - Apply -1.1V. Check that only the red light is on.

Reconnect the probe ground lead to power supply common.

CHECK PROBE OUTPUT 4-65.

Use the following procedure to check the probe output:

1. Press PROBE and select SET PROBE LOGIC LEVEL TO TTL.
2. Disconnect the probe tip from the power supply; leave the commons connected.
3. Press PROBE (twice), select OUTPUT PROBE PULSER TOGGLE, and press ENTER YES. Check that all three of the probe lights are on steady.

4. Connect an oscilloscope to the probe tip; connect the oscilloscope ground to the Clock Module COMMON. (To avoid common mode error, do not use the probe ground.)
5. Check for alternating high- and low-going pulses near a +1.8V dc level. The high output pulse should be above +4.0V (typically about +4.6V), and the low output pulse should be below +0.4V (typically about -0.6V).
6. Connect a 20-ohm resistor from the probe tip to the probe ground lead. Check that the high output pulse is +3.5V or above.
7. Connect the 20-ohm resistor from the probe tip to a +5V power supply. (Keep the probe ground lead connected to the power supply common). Check that the low output pulse is +0.8V or below.
8. To exit this test, press PROBE, select OUTPUT PROBE PULSER OFF, and press ENTER YES.

I/O Module Tests 4-66.

CALIBRATE I/O MODULE TO EXT 4-67.

Use the following procedure to calibrate the an I/O Module to EXT:

1. Press MAIN MENU, select CAL I/O MOD TO EXT, and press ENTER YES.
2. Plug the Calibration Module into the I/O Module, then press the ready button (on Calibration Module.)
3. Repeat the calibration for each I/O Module with the system.

CHECK I/O MODULE EXT SYNC 4-68.

Use the following procedure to check the I/O Module EXT sync:

1. Select SYNC I/O MOD 1 TO EXT ENABLE ALWAYS CLOCK, up arrow, START, down arrow, STOP COUNT 256, and press ENTER YES.
2. Press I/O MOD, select OUTPUT I/O MOD 1 PIN 1 HIGH LATCH, and press ENTER YES.
3. Connect the I/O Module CLOCK (yellow) and START (green) lines to a TTL signal source with a frequency between 1 kHz and 10 MHz; connect the COMMON line to the signal source common.
4. To check the I/O Module EXT sync operation, press I/O MOD (twice), ARM, and ENTER YES. Next, press I/O MOD, set SHOW I/O MOD 1 PIN 1 CAPTURED RESPONSES, and press ENTER YES. The displayed responses should be:

```
SIG= BB34     ASYNC LEVEL= 1
COUNT= 0      CLOCKED LEVEL= 1
```

5. Press I/O MOD, set OUTPUT I/O MOD 1 PIN 1 3-STATE LATCH, and press ENTER YES.
6. Repeat I/O Module EXT sync check for each I/O Module.

CHECK I/O MODULE FREQUENCY 4-69.

Using the Calibration Module lead, connect I/O Module 1 to an accurate TTL frequency source up to 10 MHz. Connect the I/O Module COMMON (black) lead to the source common. Then, use the following procedure:

1. Press I/O MOD twice, SOFT KEYS, set FREQ AT I/O MOD 1 PIN 40, and press ENTER YES. Check that the frequency read is within specification (250 ppm ±20 Hz).
2. Repeat the I/O Module frequency check with an I/O Module in each position.

CHECK I/O MODULE THRESHOLDS 4-70.

Use the following procedure to check the I/O Module thresholds:

1. Select SYNC I/O MOD 1 TO FREERUN.
2. Press I/O MOD twice, then select SET I/O MOD 1 LOGIC INPUT LEVEL TO TTL.
3. Connect the COMMON lead to the common of a variable DC power supply, with a voltmeter across the output of the power supply.
4. Apply +0.6V to the Calibration Module lead, and read the level on pin 40 by pressing I/O MOD (twice). Then set INPUT I/O MOD 1 PIN 40 and ENTER YES. Check that the display reads LEVEL = 0 (ignore the LEVEL HISTORY value displayed).
5. Apply +1.0V, then +2.1V. Read the input level for each voltage; check that LEVEL = X. Next, apply +2.6V and read the input level; check that LEVEL = 1.
6. Press I/O MOD (twice), set SET I/O MOD LOGIC LEVEL TO CMOS, and make the following checks:
   - Apply +0.8V to the Calibration Module lead, and read the level at I/O Module pin 40; check that LEVEL = 0.
   - Apply +1.2V, then +2.9V; read the level for each voltage. Check that LEVEL = X. Next, apply +3.4 V and read the input level; check that LEVEL = 1.

CHECK I/O MODULE OUTPUT 4-71.

Use the following procedure to check the I/O Module output:

1. Press I/O MOD and select SET I/O MOD LOGIC LEVEL TO TTL.
2. Disconnect the Calibration Module lead from the power supply. (Leave commons connected.)
3. Press I/O MOD (twice), select OUTPUT I/O MOD 1 PIN 40 HIGH PULSE, and press ENTER YES and LOOP.
4. Connect an oscilloscope to the Calibration Module lead; connect the oscilloscope ground to the Clock Module COMMON. (To avoid common mode error, do not use the I/O Module COMMON.) Check for high output pulses of above +2.0 V.

   For the Parallel I/O Module (9100A-003) only, connect a 24-ohm resistor from the Calibration Module lead to the I/O Module common. Check that the high output pulses are above +2.0V. Short the Calibration Module lead to the I/O Module COMMON (black) lead, and check for a repeating I/O module overcurrrent fault.
5. Press STOP and disconnect the resistor from I/O Module common.
6. Press I/O MOD, select OUTPUT I/O MOD 1 PIN 40 LOW PULSE, and press ENTER YES and LOOP. Check for low output pulses of below +0.8 V.

   For the Parallel I/O Module (9100A-003) only, connect a 33-ohm resistor from the Calibration Module lead to +5V. (The I/O Module common lead should still be connected to the power supply common.) Check that the low output pulses are

below +0.8V. Press STOP, then I/O MOD. Select OUTPUT I/O MOD 1 PIN 40 LOW LATCH, press ENTER/YES, then press LOOP. Short the Calibration Module lead to the +5V power supply output, and check for a repeating I/O module overcurrrent fault.

7. Press the STOP key, and disconnect the resistor.
8. Press I/O MOD, select OUTPUT I/O MOD 1 PIN 40 3-STATE LATCH, and press ENTER YES.
9. Repeat the I/O Module threshold and output checks for each I/O Module.

CHECK I/O MODULE DATA COMPARE EQUAL (DCE) 4-72.

Use the following procedure to check the I/O Module DCE:

1. Press I/O MOD and select OUTPUT I/O MOD 1 WORD 1 DATA 0 LATCH.
2. Press I/O MOD, select SET I/O MOD 1 COMPARE WORD 1 TO 5555555555 (ten 5's), and press ENTER YES.
3. Select OUTPUT I/O MOD 1 WORD 1 DATA 5555555555 LATCH, and press ENTER YES. Check that a 'compare condition reached in I/O module 1' fault occurs.
4. Press I/O MOD, select SET I/O MOD COMPARE WORD 1 TO AAAAAAAAAA, and press ENTER YES.
5. Set OUTPUT I/O MOD 1 WORD 1 DATA AAAAAAAAAA LATCH, and press ENTER YES. Check that a 'compare condition reached in I/O module 1' fault occurs again.
6. Enter OUTPUT I/O MOD 1 WORD 1 3-STATE MASK FFFFFFFFFF, and press ENTER YES.
7. Repeat the I/O Module DCE check for each I/O Module.

Check Floppy Disk Drive Operation 4-73.

Insert a write-enabled floppy disk into the floppy disk drive. (On a 9105FT, use DR1, the top drive.) Note that any data on the floppy disk will be erased.

1. Press MAIN MENU twice, then press SOFT KEYS.
2. Select FORMAT DISK IN DR1 (do not press ENTER YES at this point.)
3. If the menu displays DENSITY, select HIGH and insert a high density (HD type) floppy disk in the floppy disk drive. Otherwise, insert a standard double density (DD type) disk.
4. Press ENTER YES. The BUSY light will go off when the floppy disk format is complete (the format will take several minutes.)
5. On the 9105FT, repeat the floppy disk format with DR2 (the bottom drive.)

Check Floppy Disk Read/Write 4-74.

With the floppy disk formatted in the previous step in the disk drive (top drive on 9105FT), use the following procedure to check read/write operation:

1. Press MAIN MENU twice, then press SOFT KEYS.
2. Select COPY DR1 TO DR1 and press ENTER YES.
3. When the display prompts to insert the source disk, press ENTER YES again.

4. When the display prompts to insert the write-enabled empty disk, press ENTER YES; do not remove or change the floppy disk. The disk copy function will take several minutes.

5. Press ENTER YES each time the display prompts to insert the disks again. Check that the disk copy is completed with no errors.

Check Disk Change Operation 4-75.

Use the following procedure to check disk change operation:

1. First remove the disk from the floppy disk drive, then reinsert a formatted disk in the drive. Press SETUP MENU and select SETUP USERDISK DR1.

2. Now press EXEC and HELP, and check that the light on the floppy disk drive comes on for several seconds. Press CLEAR NO and ALPHA.

3. Remove and reinsert the disk. Press EXEC and HELP, and check that the floppy drive light comes on again. Press CLEAR NO and ALPHA.

4. On the 9105FT, repeat steps 1, 2, and 3 on DR2.

Check Serial Port Operation 4-76.

Use the following procedure to check serial port operation:

1. Disconnect the pod from the UUT or self test socket, leaving the cable(s) unconnected. (The pod should still be connected to the 9100FT or 9105FT.)

2. Using a Null Modem cable, connect an RS-232 terminal to the serial Port 1 connector on the rear panel.

3. Set up the terminal to 9600 baud, no parity, 8 data bits, and 1 stop bit, to match the default 9100FT/9105FT settings.

   An alternative procedure allows you to press SETUP MENU and use SETUP PORT1 to set the mainframe's serial port to match the terminal. If the serial port 1 setup is changed, be sure that SETUP PORT1 XON/XOFF is still set to ENABLE.

4. Press MAIN MENU twice, the MODE softkey, and the TEST softkey.

5. Then select MAIN: MODE TEST BY CONTINUING WITH FAULTS TO PORT1 and press ENTER YES.

6. Force a fault by pressing READ ADDR 0 and ENTER YES. Check that a fault message is sent from the serial port to the terminal; typical messages would be "pod timeout bad UUT power supply" or "attempted to READ @ 0". Type Ctrl-S on the terminal keyboard (hold the Ctrl key and type S).

7. Press ENTER YES on the 9100FT/9105FT; check that no new fault message is sent to the terminal. Then, type Ctrl-Q on the terminal keyboard, and verify that the fault message is sent by the 9100FT/9105FT serial port.

8. Repeat the serial port operation check with Port 2.

Check IEEE-488 Operation 4-77.

An IEEE-488 controller is needed to check IEEE-488 Interface operation. A Fluke 1722A Instrument Controller is used in the following verification procedure:

1. On the 9100FT/9105FT, select IEEE-488 operation with the following key sequence:

SETUP MENU right arrow SOFT KEYS IEEE (softkey)

Then, select talk/listen mode with the following key sequence:

right arrow FUNCTION (softkey) right arrow TLK/LST (softkey)

Finally, select the address with the following procedure:

ADDRESS (softkey) right arrow 0 ENTER YES

2. Enter BASIC on the 1722A. Connect an IEEE-488 cable from the “IEEE STD-488” connector on the left side of the 9100FT/9105FT mainframe to the IEEE PORT 0 connector on the 1722A.

CHECK ‘GO TO REMOTE’ 4-78.

Initialize the IEEE-488 port and put the 9100FT/9105FT into remote at address 0. On the 1722A, do this by typing the following:

```
INIT PORT 0
REMOTE @0
```

NOTE

End each line with the (RETURN) key. The 1722A should return ‘Ready’ with no error after each line is sent.

The 9100FT/9105FT operator’s display should now read ‘REMOTE CONTROL IN PROCESS’.

CHECK REMOTE OPERATION 4-79.

Send the remote command ‘*IDN’ (IDeNtification query) to the 9100FT/9105FT, then read the serial poll response. On the 1722A, do this by typing the following:

```
PRINT @0, “*IDN?”
PRINT SPL(0)
```

The 1722A should now display ‘16’ (the serial poll response in decimal, binary = 00001000)), followed by ‘Ready’.

CHECK REMOTE DATA TRANSFER 4-80.

Read the IDeNtification query string from the 9100FT/9105FT. Do this on the 1722A by typing the following:

```
INPUT LINE @0, A$
PRINT A$
```

The 1722A should now display ‘FLUKE’, followed by the 9100FT/9105FT mainframe model, serial number, and software version.

Read the serial poll response again by typing the following on the 1722A:

```
PRINT SPL(0)
```

The 1722A should now display the serial poll response ‘0’.

This completes the 9100FT/9105FT performance test.

CALIBRATION 4-81.

Individual level and time delay variations associated with the Probe, I/O Module, and Pod can be compensated for with the calibration adjustments presented in the following paragraphs. The following six calibrations are covered:

- Probe offset correction calibration
- Probe compensation calibration
- Probe to external clock module calibration
- Probe to Pod calibration
- I/O Module external calibration
- I/O Module to Pod calibration

The calibrations listed above fall into three categories. Offset correction calibration stores a correction value in non-volatile memory, Compensation calibration matches impedances. Data against clock delay calibration, performed in software, ensures that both data and the signal clocking the data arrive at the receiving hardware at the same time.

Probe compensation remains stable and is necessary only when a Probe is first connected to the mainframe. The software calibration procedures are intended to be performed by the system operator and do not require any test equipment.

Software calibration should be performed when the system is first set up and at regular intervals (at least monthly) thereafter. Calibration is also necessary whenever devices attached to the system are changed or repaired.

The system can also be calibrated by restoring data generated by previous calibrations. This process, described under “Saving and Restoring Calibration Data” later in this section, should be performed after each power-up or reset and before UUT testing or troubleshooting.

Probe Offset Correction 4-82.

Probe offset correction calibration calculates the offset voltage of the Probe input circuitry and stores the value in an EEPROM. This procedure is required only if the Probe I/O-ECL or Main PCAs are repaired or replaced.

A utility program is required to perform the probe offset correction calibration. This utility program is included on the 9100 Series Utility Disk, which is part of the 9100FT Service Kit (see Troubleshooting).

Probe Compensation 4-83.

This calibration procedure matches the impedance of the Probe to that of the system. Probe impedance is adjusted with COMP ADJ, a trimmer capacitor located on the side of the system.

Figure 4-8 shows oscilloscope connections used during probe compensation. To compensate the Probe, use the following steps:

1. Ensure that the oscilloscope and its probe are properly compensated.
2. Connect the oscilloscope probe tip to the system CAL OUT test point. Then connect the oscilloscope probe common to the system COMMON test point. Both test points are accessible through labeled holes in the right side of the mainframe.

3. Press the MAIN MENU key, and use the left arrow key to move the cursor to the left-most field.

4. Press the CAL softkey.

5. Use the right arrow key to move the cursor to the next field, and press the PROBE softkey.

6. Move the cursor to the next field, and press the COMP softkey. The display should now read:

```
MAIN: CAL PROBE COMP
```

7. Press the ENTER key. The display should read:

```
MAIN: CAL PROBE COMP
CONNECT PROBE TO TRIGGER OUTPUT
ADJUST COMP, PRESS STOP WHEN DONE
```

8. Insert the probe tip into the central (innermost) conductor of the TRIGGER OUTPUT at the rear of the 9100FT/9105FT. Leave the Probe in this position.

9. Adjust the oscilloscope's horizontal and vertical settings until an approximate square wave is displayed. Then use an adjustment tool on COMP ADJ to obtain an underdamped square wave with 10% overshoot. For the adjustment tool, use Fluke Part Number 800540. The square wave should bear similarity to Figure 4-9.

10. When you have finished the square wave adjustment, press the STOP key on the operator's keypad. The display should read:

```
MAIN: CALIBRATION COMPLETE
```

Software Calibration 4-84.

The Probe Compensation adjustment and the Probe Offset Calibration are the only hardware calibrations required for the 9100FT/9105FT. All other calibration is performed in software and is lost if the system is turned off, restarted, or reset. The software calibration data can be saved on disk and restored from disk to recalibrate the system. However, the restored calibration data must only be used with the system on which the calibration was performed. Any change in system hardware (Interface Pod, I/O Module(s) Clock Module, or Probe) requires system recalibration; the resulting new calibration data should be saved.

All of the software calibration procedures are intended to be performed by the system operator and do not require test equipment. Pod-related calibration procedures require the use of a known good Unit Under Test (UUT).

PROBE TO EXTERNAL CALIBRATION (CLOCK MODULE) 4-85.

This calibration automatically calibrates the Probe's internal data delay to the external clock delay. The clock signal input is through the Clock Module, which must be connected to the system. Perform the calibration as follows:

1. Press the MAIN MENU key, and use the left arrow key to move the cursor to the left-most field.

2. Press the CAL softkey.

3. Move the cursor to the next field, and press the PROBE softkey.

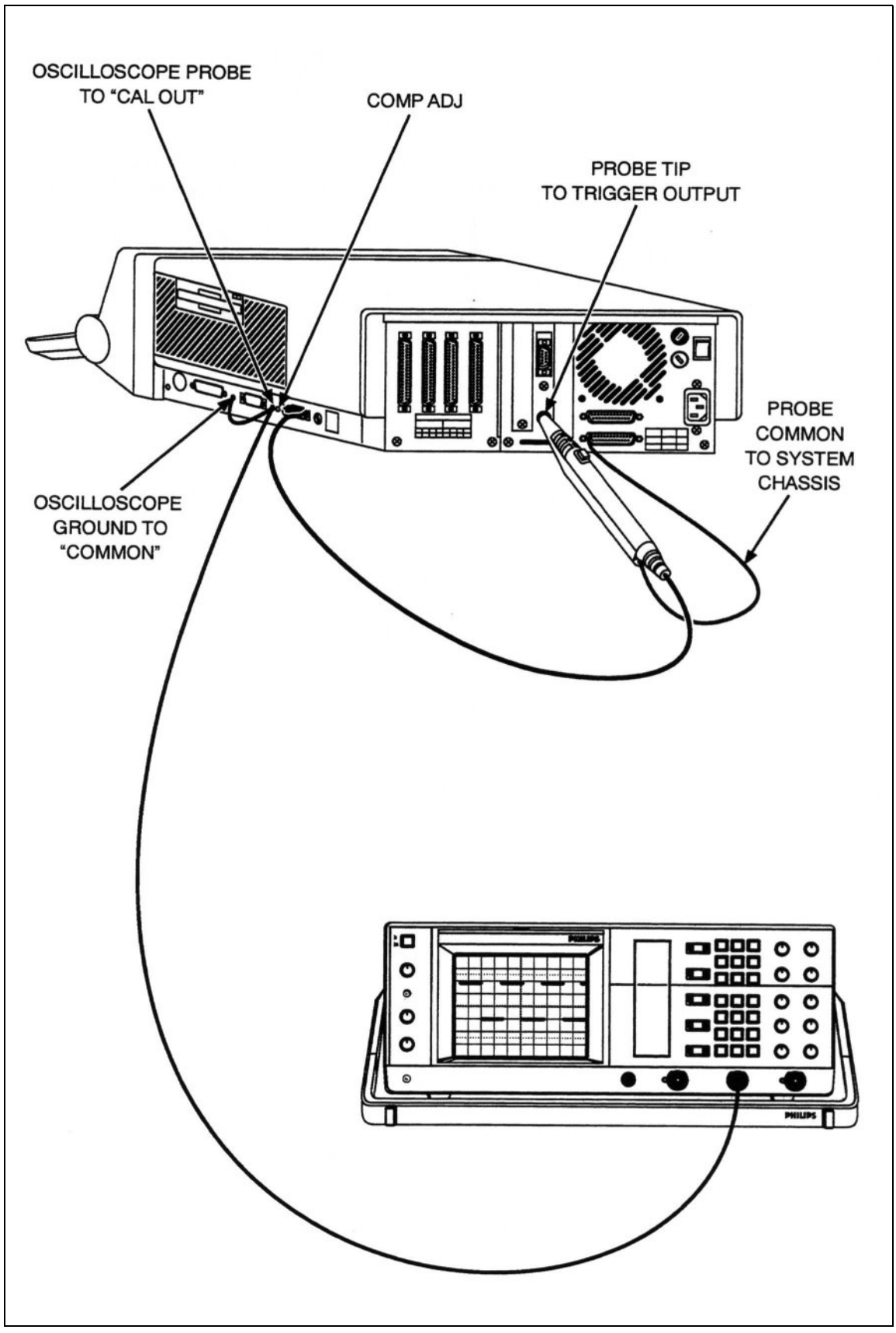


Figure 4-8. Oscilloscope Use in Probe Compensation

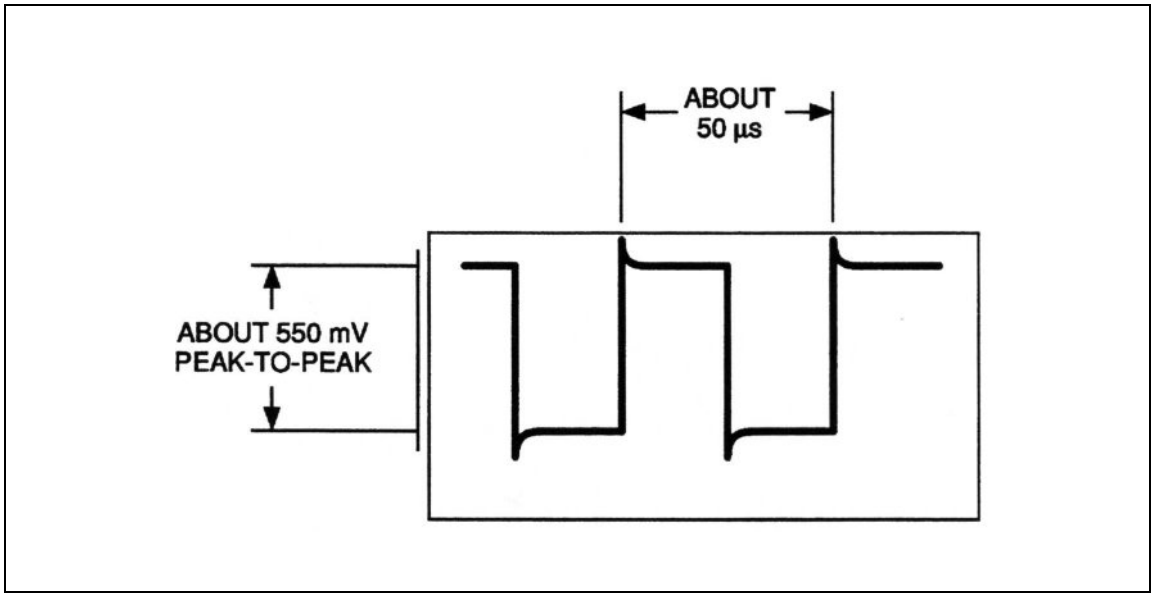


Figure 4-9. Probe Compensation Square Wave

4. Move the cursor to the next field, and press the TO EXT softkey. The display should read:

```
MAIN: CAL PROBE TO EXT
```

5. Press the ENTER key. The display should read:

```
MAIN: CAL PROBE TO EXT
```

6. Connect the Probe to the Clock Module CLOCK line.

7. Connect the probe ground clip to the Clock Module COMMON line.

8. Press the probe ready button (side of Probe). The display should read:

```
MAIN: CALIBRATION COMPLETE
```

PROBE TO POD CALIBRATION 4-86.

This procedure automatically calibrates the Probe's internal data delay to the Pod's PodSync line, which the system sometimes uses as a clock signal. Use the following steps to perform the calibration:

1. Connect the Pod to a UUT.

2. Press the MAIN MENU key, and use the left arrow key to move the cursor to the left-most field.

3. Press the CAL softkey.

4. Move the cursor to the next field, and press the PROBE softkey.

5. Move the cursor to the next field, and press the TO POD softkey. The display should read:

```
MAIN: CAL PROBE TO POD ADDR
```

The last field is pod dependent and softkey selectable.

6. Press the ENTER key. The display asks you to probe the UUT at a point where the selected PodSync appears. The message is pod dependent, a possible example being:

```
MAIN: CAL PROBE TO POD ADDR
 CONNECT PROBE TO ALE
 PRESS PROBE BUTTON WHEN READY
```

7. Connect the probe common clip to the UUT common.

8. Probe the specified pod line as directed. You may need to refer to the UUT schematic for convenient probing locations.

9. With the probe tip touching the point being probed, push the probe ready button.

10. You may have to repeat steps 8 and 9, probing at different locations each time. When calibration is complete, the display should read:

```
MAIN: CALIBRATION COMPLETE
```

11. Repeat steps 5 through 10 for each SYNC mode in which the 9100FT/9105FT is to be operated.

I/O MODULE TO EXTERNAL CALIBRATION 4-87.

This procedure calculates the proper setting for the I/O Module's internal clock delay for use whenever the SYNC I/O MOD TO EXT command is entered. This calibration requires the use of the Calibration Module supplied with the I/O Module. To perform the calibration:

1. Press the MAIN MENU key, and use the left arrow key to move the cursor to the left-most field.

2. Press the CAL softkey.

3. Move the cursor to the next field, and press the I/O MOD softkey.

4. Move the cursor to the next field, and press the EXT softkey. The display should read:

```
MAIN: CAL I/O MOD TO EXT
```

5. Press the ENTER key. The display should read:

```
MAIN: CAL I/O MOD TO EXT
 INSTALL CAL HEADER IN DESIRED I/O MODULE
 PRESS BUTTON WHEN READY
```

6. Fit the Calibration Module over the I/O Module to be tested.

7. Press the ready button on the Calibration Module. When the calibration is complete, the BUSY light should go off, and the display should read:

```
MAIN: CALIBRATION COMPLETE
```

I/O MODULE TO POD CALIBRATION 4-88.

This procedure calculates the proper settings for the I/O Module's internal clock delay for use with the SYNC I/O MOD TO EXT and the SYNC I/O MOD TO POD commands. When either is entered, the appropriate delay is selected. This calibration procedure requires use of the Calibration Module. Perform the calibration as follows:

1. Connect the Pod to a UUT.
2. Press the MAIN MENU key, and use the left arrow key to move the cursor to the left-most field.
3. Press the CAL softkey.
4. Move the cursor to the next field, and press the I/O MOD softkey.
5. Move the cursor to the next field, and press the POD softkey.
6. Move the cursor to the next field, and press the desired softkey. For example, if you intend to use the 9100FT/9105FT in SYNC I/O MOD TO POD ADDR mode, press the ADDR softkey. In this case, the display should read:

```
MAIN: CAL I/O MOD TO POD ADDR
```

7. Press the ENTER key. This display should read:

```
MAIN: CAL I/O MOD TO POD ADDR
 INSTALL CAL HEADER IN DESIRED I/O MODULE
 PRESS BUTTON WHEN READY
```

8. Plug the Calibration Module into the I/O Module, and press the Calibration Module ready button. Make sure the calibration lead on the Calibration Module is unconnected when pressing the ready button.
9. After a few seconds, a pod dependent message is displayed. For example, the display may read:

```
COMPLETED EXT CAL PRIOR TO CAL POD
 NOW CONNECT CAL LEAD TO ~Sl
 PRESS BUTTON WHEN READY
```

10. Refer to a schematic of the UUT and locate the specified signal. At a suitable point on the UUT, attach the calibration lead to this signal.
11. Press the Calibration Module ready button. After several seconds, the display should read:

```
MAIN: CALIBRATION COMPLETE
```

12. Repeat steps 6 through 11 for each SYNC mode in which the 9100FT/9105FT is to be operated.

SAVING AND RESTORING CALIBRATION DATA 4-89.

Calibrating the 9100FT/9105FT at every power-up or reset is not necessary. A more convenient procedure is to restore calibration data from the user disk after the self tests have been performed and the system configured.

Each calibration generates data, which can be saved on the user disk using the SETUP MENU key. Once the system is calibrated for a given Pod, Probe, Clock Module, and I/O Module, the data is good until one or more of those devices is changed.

Invalid Calibration Data 4-90.

The calibration data restored from the user disk may be invalid if any of the following conditions apply:

- After the data was saved, one or more system components (Pod, Probe, I/O Module, Clock Module) were changed. This condition includes moving or exchanging I/O Modules, such as moving an I/O Module from connector 1 to connector 2.

- The system has never been calibrated.
- The system was last calibrated more than one month ago.

Saving Calibration Data 4-91.

Save calibration data on the disk as follows:

1. Press the SETUP MENU key, and use the left arrow key to move the cursor to the left-most field.
2. Press the SAVE softkey.
3. Move the cursor to the next field, and press the CALDATA softkey.
4. Move the cursor to the next field. Press the USERDISK softkey if the user disk does not contain a UUT directory. The resulting display should read:

   ```
   SAVE CALDATA IN USERDISK
   ```

   Press the UUT FILE softkey if the user disk contains a directory for the UUT.
5. If you pressed the UUT FILE softkey in step 4, type the UUT directory name. For example, type DEMO. The display should read:

   ```
   SAVE CALDATA IN UUT FILE DEMO
   ```
6. Press ENTER to save calibration data.

Restoring Calibration Data 4-92.

Use the following procedure to restore calibration data from a user disk:

1. Press the SETUP MENU key, and use the left arrow key to move the cursor to the left-most field.
2. Press the RESTORE softkey.
3. Move the cursor to the next field, and press the CALDATA softkey.
4. Move the cursor to the next field. Press the USERDISK softkey if the calibration data was saved in the USERDISK directory. The resulting display should read:

   ```
   RESTORE CALDATA FROM USERDISK
   ```

   Use the UUT FILE softkey if the calibration data was saved in a UUT directory.
5. If you pressed the UUT FILE softkey in step 4, type the UUT directory name. For example, type DEMO. The display should read:

   ```
   RESTORE CALDATA FROM UUT FILE DEMO
   ```
6. Press ENTER to restore the previously saved calibration data.

TROUBLESHOOTING 4-93.

This manual does not contain troubleshooting procedures. Component level troubleshooting is supported by the 9100FT Service Kit, P/N 897116. The Service Kit uses programs to assist in troubleshooting 9100FT/9105FT systems. The Service Kit contains troubleshooting and utility programs and instructions. To use the Service Kit, another 9105FT or 9100FT, an I/O Module (9100A-003), and a 9132FT Memory Interface Pod with 9132FT-68030 Processor Support Package are required.

REPAIR 4-94.

General Repairs 4-95.

STATIC AWARENESS 4-96.

Improper handling of components or assemblies may cause instantaneous or delayed electrostatic discharge damage. The yellow “Static Awareness” sheet inserted near the front of this manual explains some of the hazards associated with static electricity and sensitive components.

COMPONENTS 4-97.

Several of the assemblies in the 9100FT/9105FT are built with surface mount components. See the following Surface Mount Repair information concerning mechanical design and repair of these components.

Surface Mount Repair 4-98.

The 9100FT/9105FT incorporates Surface-Mount Technology (SMT) for printed circuit assemblies (pca’s). Surface-mount components are much smaller than their predecessors, with leads soldered directly to the surface of a pca; no plated through-holes are used. Unique servicing, troubleshooting, and repair techniques are required to support this technology. The information offered in the following paragraphs serves only as an introduction to SMT. It is not recommended that repair be attempted based only on the information presented here. Refer to the Fluke “Surface Mount Device Soldering Kit” for a complete demonstration and discussion of these techniques.

Since sockets are seldom used with SMT, “shotgun” troubleshooting cannot be used; a fault should be isolated to the component level before a part is replaced. Surface-mount assemblies are probed from the component side. The probes should make contact only with the pads in front of the component leads. With the close spacing involved, ordinary test probes can easily short two adjacent pins on an SMT IC.

This Service Manual is a vital source for component locations and values. With limited space on the pca, chip component locations are seldom labeled. Figures provided in Section 5 of this manual provide this information. Also, remember that chip components are not individually labeled; keep any new or removed component in a labeled package.

Surface-mount components are removed and replaced by reflowing all the solder connections at the same time. Special considerations are required.

- The solder tool uses regulated hot air to melt the solder; there is no direct contact between the tool and the component.
- Surface-mount assemblies require rework with wire solder rather than with solder paste. A 0.025-inch diameter wire solder composed of 63% tin and 37% lead is recommended. A 60/40 solder is also acceptable.
- A good connection with SMT requires only enough solder to make a positive metallic contact. Too much solder causes bridging, while too little solder can cause weak or open solder joints. With SMT, the anchoring effect of the through-holes is missing; solder provides the only means of mechanical fastening. Therefore, the pca must be especially clean to ensure a strong connection. An oxidized pca pad causes the solder to wick up the component lead, leaving little solder on the pad itself.

Refer to the Fluke “Surface Mount Device Soldering Kit” for a complete discussion of these techniques.

FT MAIN PCA 4-99.

The FT Main PCA almost exclusively uses surface mount technology. Many of the other assemblies in the 9100FT/9105FT mainframe connect directly to the Main PCA. These assemblies include the Power Supply, Floppy Disk Drive(s), RAM Modules, Display PCA, Probe I/O-ECL PCA, Multi-Function Interface II PCA, and Video Controller PCA. The fan and serial Ports 1 and 2 plug into the Main PCA. Also, an Interface Pod and the Programmer's Keyboard plug into external connectors on the Main PCA.

The FT Main PCA includes an EEPROM, U8, that contains characterizing data for the instrument and stores certain parameters. If this EEPROM is to be replaced, the replacement must be ordered as a programmed part. Certain characteristics must be programmed into it after the replacement EEPROM is installed; this can be done by a Fluke Technical Center, or with a utility program that is included with the 9100FT Service Kit. Also, certain other hardware changes require that the EEPROM be reprogrammed.

CAUTION

When reinstalling the Main PCA (or rear panel) take care to connect the cables from the RS-232 ports to the correct connectors on the pca. Improper connections can cause a short to earth ground. Proper connections are: RS-232 Port 1 to J16 on the Main PCA and RS-232 Port 2 to J14 on the Main PCA.

DISPLAY AND KEYPAD 4-100.

The Display Interface PCA uses surface mount technology. The Keypad PCA connects to the Display Interface PCA.

Display and Keypad PCAs have several built in self tests and diagnostics; these are described under "Display Self Test" earlier in this section. The self tests allow checking and some troubleshooting of the display and operator keypad functions.

The Display Interface PCA contains a vacuum fluorescent display tube. This display tube has a glass envelope and is susceptible to breakage. Caution should be taken to prevent sharp blows or direct pressure to the glass envelope or to leads of the vacuum fluorescent tube.

The display tube is driven with high voltage (approximately 70 volt pulses at the grids and anodes). Attempting to measure the outputs of the driving circuitry or the inputs to the display tube with a logic probe or other low voltage measuring device can cause equipment damage.

The Keypad PCA's only active components are the key switches and a single light-emitting diode.

PROBE I/O 4-101.

The Probe I/O-ECL PCA uses surface mount technology extensively. It includes several custom LSI components. The I/O Connector PCA and Trigger Output connector plug into this assembly. The Clock Module, Single-Point Probe, and the External Switch plug into external connectors. The Probe fuse holder is also mounted on the Probe I/O-ECL PCA.

The Probe I/O-ECL PCA contains the logic probe signal input circuitry. Changes to portions of this circuitry cause calibration changes. Probe compensation should be performed after any changes in the probe input circuit, including replacing or changing the Single-Point Probe. Any changes in the probe input, probe threshold, or DAC (digital to analog) circuits require reprogramming the probe offset level in the EEPROM (U11 on the Main PCA); this can be done by a Fluke Technical Center, or with a utility program that is included with the 9100FT Service Kit.

I/O CONNECTOR 4-102.

There is no special repair information for the I/O Connector PCA.

SINGLE-POINT PROBE 4-103.

The Single-Point Probe primarily uses surface mount technology. Repair or replacement of the probe, or use of another probe, requires that the probe compensation adjustment be performed.

CLOCK MODULE 4-104.

The Clock Module is partially based on surface mount technology.

When reinstalling the Clock Module case or flying lead wires, take care to install them correctly. The case should be installed with the signal name “COMMON” next to the black lead wire; the flying lead wires should be installed with the black lead wire on the same side of the assembly as the fuse holder. Remember to install the plug in the case hole (opposite the fuse holder).

RAM MODULES 4-105.

The 9100FT/9105FT uses either 1M byte or 4M byte SIP DRAM modules. The RAM modules plug into the Main PCA. The RAM Address Switches on DIP switch S1 must be set correctly for the RAM module combination installed. See Table 4-4 for the correct settings. If a new RAM configuration is installed, the EEPROM must be reinitialized by a Fluke Service Center or by using a utility program included with the Service Kit.

POWER SUPPLY 4-106.

The Power Supply is an OEM assembly and is replaced as a single part. The Power Supply is a switching supply and should not be operated without the correct load.

The power supply has one user adjustment. The +5 volt supply can be adjusted for the correct voltage. Adjust R44, if necessary, for a +5V supply voltage of +5.1V ± 0.01V with a normal load. No other power supply adjustments should be attempted.

Table 4-4. RAM Configuration

RAM COMPLEMENT	TOTAL BYTES	ADDRESS RANGE	S1 SWITCH SEGMENTS 1234 5678
1 BANK of 1M Byte SIMM	4M	100000-4FFFFF	XXXX 01XX
2 BANKS of 1M Byte SIMM	8M	100000-8FFFFF	XXXX 10XX
1 BANK of 4M Byte SIMM	15M	100000-FFFFFF	XXXX 01XX
			1 = ON (closed) 0 = OFF (open)

The other power supply voltages should measure, with a normal load, as follows:

- The +12V supply should be +12V ± 0.5V.
- The +12VN supply should be +12V ± 1.0V.
- The -5V supply should be -5V ± 0.25V.

FLOPPY DISK DRIVE 4-107.

The Floppy Disk Drive is an OEM assembly and is replaced as a single part. The Drive Select Switch (located on right rear side of disk drive) must be set for Drive 1 (“0” setting) on the 9100FT/9105FT or Drive 2 (“1” setting) on the 9105FT only. When a floppy disk drive or hard disk drive is replaced with a different type, the EEPROM must be reinitialized. This procedure can be carried out by a Fluke Service Center or by using a utility program included with the Service Kit.

HARD DISK 4-108.

The Hard Disk Drive is an OEM module. The hard disk is mechanically fragile. It should be allowed to “park” itself before the instrument is turned off or moved. The disk drive parks ten seconds after the last disk access; the DISK ACCESS light on the display flashes once when it parks. Shaking or jarring of the disk drive while it is operating or before it has parked can damage the drive and cause loss of data on the disk.

Because the Hard Disk can easily be damaged by incorrect operation, it is good practice to disconnect the hard disk when troubleshooting a non-functional 9100FT. To do this, unplug the power connector from the drive before turning on the 9100FT power.

A replacement hard disk must be formatted before the operating software and user data can be loaded. The disk can be formatted with the Service Utility Program in the 9100FT Service Kit, or the hard disk can be ordered pre-formatted.

The operating software can be loaded on a formatted hard disk even if the 9100FT is not able to boot up from the hard disk. Use the following procedure:

1. Put the System Disk 1 floppy disk in the floppy disk drive.
2. Hold down the three keys SOFT KEYS, F2, and F4, then turn on the 9100FT power (or press the Restart button on the right side panel if the power is already on).
3. When the display message indicates that it is booting from the floppy disk, release the three keys.
4. Change to the next System Disk when instructed by the display.
5. When the 9100FT displays the READY message, the software can be loaded on the hard disk by using the COPY function in the Main Menu to copy the System and User disks (and Programmer’s software, if applicable) from the floppy disks to the hard disk. See Section 3 of the Technical User’s manual for more information on copying disks.

MULTI-FUNCTION INTERFACE 4-109.

The Multi-Function Interface II PCA plugs into J11 on the FT Main PCA (the 96-pin connector on the right). The Hard Disk is connected through a cable to a connector on the Multi-Function Interface II PCA. The assembly also contains the IEEE-488 interface, the Direct Memory Access (DMA) circuit, and the Real-Time Clock.

VIDEO CONTROLLER 4-110.

The Video Controller PCA uses mainly surface mount technology. The Monochrome Video Interface and the Color Video Interface use the same assembly, with jumpers to select the mode. The Video Controller plugs into J12 on the FT Main PCA (the 64 pin connector between J11 and J13); it has an external connector that passes through the rear panel for connection to a monitor.

For the Monochrome Video Interface, jumper block Z1 is installed on the Video Controller PCA; jumper block Z2 is installed for the Color Video Interface.

MONOCHROME MONITOR 4-111.

The Monochrome Monitor contains two OEM modules. The power supply is an OEM module that is replaced as a single part. The CRT and Video Display PCA is an OEM set; both the CRT and Video Display PCA are replaced at the same time.

PARALLEL I/O MODULE 4-112.

The Parallel I/O Module consists of two assemblies. The I/O Main PCA uses surface mount technology, with components mounted on both sides of the pca. The I/O Module Top PCA has interface connectors and a few other components.

Repair of the I/O Main PCA, which has SMT components mounted on both sides, is performed in the same way as with other SMT assemblies, except that extra care needs to be taken not to overheat the pca. Too much heat applied to one side could cause nearby components on the other side to pull away from the pads or fall off the pca.

Replacing the external mating connectors on the I/O Module Top PCA must be done carefully. The connectors are a high-reliability type, designed for a large number of insertion/removal cycles. Alignment of the connectors is critical to allow proper mating with the external interface modules. When replacing the connectors, align them in the same way as the mating connectors on the Clip or Flying Lead modules, below, using a full width interface module as an alignment fixture.

CLIP OR FLYING LEAD MODULES 4-113.

The Clip Module and Flying Lead Module interface the I/O modules to a Unit Under Test (UUT) using IC clips or flying leads. They are either half width modules, for up to 24 pins, or full width modules, for up 40 pins. The Calibration Module (used for software calibration of the I/O Module) is similar to the full width modules.

The Clip and Flying Lead modules use internal configuration switches that are read by the I/O Module to determine the type of module attached. The half-width modules use a four-bit switch, and the full-width modules use an eight-bit switch. See Table 4-5 for a list of switch settings. When servicing a Clip or Flying Lead Module, be sure that the configuration switches are set correctly.

The connectors and connector alignment posts that mate the Clip or Flying Lead modules to the I/O Module must be aligned precisely with the mating connectors on the I/O Module. Use the following procedure when installing the connectors:

1. Make sure the solder is removed from all the holes for the connector before attempting to install it. The connector should fit loosely in the holes.

2. Place the connector in the holes in the pca, and place the connector posts though the large holes in either end. Be sure that the notches on the posts line up correctly.

Table 4-5. Clip and Flying Lead Module Configuration Switch Settings

BIT SWITCHES 8765 4321	MODULE
0000	14-Pin Clip
0001	16-Pin Clip
0010	18-Pin Clip
0011	20-Pin Clip
0100	24-Pin Clip
1101	20-Pin Flying Lead Set
1110 0000	28-Pin Clip
1110 0001	40-Pin Clip
1110 0010	Calibration Module (hardwired)
0 = on (closed) 1 = off (open)	

3. Put on the nuts or screws loosely enough that the connector can move somewhat. Use an I/O Module as an alignment fixture; gently plug the module being repaired into an I/O Module, taking care that the connectors mate correctly. With the connectors completely seated, tighten the nuts or screws, and solder several pins on the connector (and the alignment posts, if necessary) to hold it in place. The module being repaired can be unplugged to solder the remaining pins.

OEM Assemblies 4-114.

Some of the assemblies in the 9100FT/9105FT are Original Equipment Manufacturer (OEM) modules; each of these modules is treated as a single part. This Service Manual does not contain component level parts lists for these modules, since they are not manufactured or supported to the component level by Fluke.

Section 5
List of Replaceable Parts

INTRODUCTION 5-1.

Section 5 provides an illustrated parts list for the 9100FT, 9105FT, and related optional assemblies.

Components are listed alphanumerically by assembly. Both electrical and mechanical components are listed by reference designation. Each listed part is shown in an accompanying illustration.

The parts lists contain the following information:

- Reference Designator
- Description
- Fluke Stock Number
- Federal Supply Code for Manufacturers (MFRS SPLY CODE)
- Manufacturer's Part Number
- Total Quantity of Components per Assembly (TOT QTY)

HOW TO OBTAIN PARTS 5-2.

Use the Fluke Stock Number when ordering all components from the John Fluke Mfg. Co., Inc. or an authorized representative. In the U.S., order directly from the Fluke Parts Dept. by calling 1-800-526-4731.

Some components may be ordered directly from the manufacturer using the manufacturer's part number. See the code-to-name list at the end of this section.

In the event that the part you order has been replaced by a new or improved part, the replacement will be accompanied by an explanatory note and installation instructions, if necessary.

To ensure prompt and efficient handling of your order, include the following information.

1. Instrument Model, Serial Number, and Instrument Firmware Numbers
2. Fluke Stock Number
3. Reference Designator
4. Printed circuit assembly (pca) part number and revision letters
5. Description
6. Quantity

Price information for parts is available from the John Fluke Mfg. Co., Inc., and its authorized representatives. Prices are also available in a Fluke Replacement Parts Catalog, which is available on request.

CAUTION

The symbol ↯ indicates a device that may be damaged by static discharge.

TECHNICAL SERVICE CENTERS 5-3.

Refer to the end of this section for a list of technical service centers.

MODEL CONFIGURATIONS 5-4.

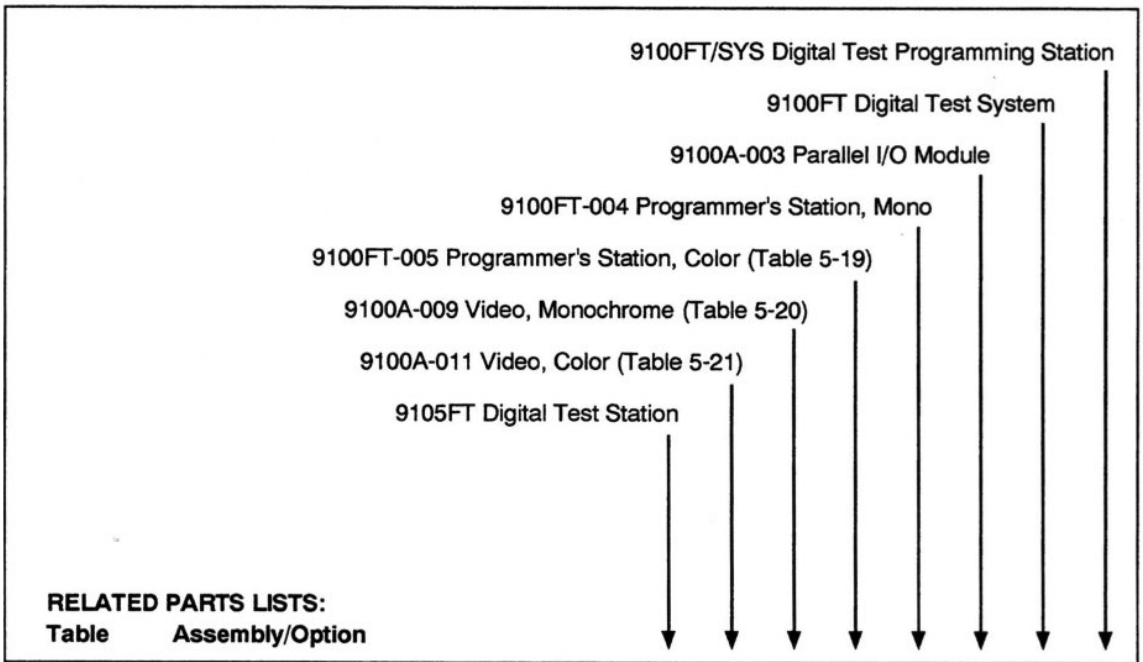
Figure 5-1 identifies the parts lists applicable to your 9100 Series model.

MANUAL STATUS INFORMATION 5-5.

Assembly revision levels are documented in the "Manual Status Information" table later in this section. To identify the configuration of the pca's used in your instrument, refer to the revision letter (marked in ink) on the component side of each pca.

NEWER INSTRUMENTS 5-6.

Changes and improvements made to the instrument are identified by incrementing the revision letter marked on the affected pca. These changes are documented on a supplemental change/errata sheet which, when applicable, is inserted at the front of the manual.



RELATED PARTS LISTS: Table	Assembly/Option							
5-1	Final Assembly	X						X	X
5-2	A1 Main PCA	X						X	X
5-3	A2 Display Interface PCA	X						X	X
5-4	A4 Video Controller PCA		X	X	X	X			X
5-5, 5-5A	A5 Probe PCA and Accessories	X						X	X
5-6	A6 Clock Module PCA	X						X	X
5-7	A7 I/O Module (Main) PCA						X		X
5-8	A8 I/O Module (Top) PCA						X		X
5-9	A11 I/O Connector PCA	X						X	X
5-10	A12 Half-Width Clip Module								X
5-11	A13 Full-Width Clip Module								X
5-12	A14 Calibration Module						X		X
5-13	A15 Flying Lead Module						X		X
5-14	A19 Monochrome Monitor			X		X			X
5-15	A24 Multi-Function I/F II PCA	X						X	X
5-16	A25 Probe I/O-ECL PCA	X						X	X
5-17	-003 Parallel I/O Module								X
5-18	-004 Programmer's Station, Mono								X

Figure 5-1. Model Configurations

Manual Status Information

REF	ASSEMBLY NAME	FLUKE PART NO	REVISION LEVEL
A1	FT Main PCA	890660	C1
A2	Display IF PCA	768689	D
A3	Keypad	846357	D
A4	Video Controller PCA	768762	D
A5	Probe PCA	773911	F
A6	Clock Module PCA	768812	B1
A7	I/O Module (Main) PCA	768838	F1
A8	I/O Module (Top) PCA	755611	A2
A11	I/O Connector PCA	767996	B
A24	Multi-Function I/F II PCA	877808	D
A25	Probe I/O-ECL PCA	778118	B

Table 5-1. 9100FT Series Final Assembly

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
A 1	✓ MAIN PCA	890660	89536	890660	1	
A 2	✓ DISPLAY INTERFACE PCA	768689	89536	768689	1	
A 3	✓ KEYPAD ASSEMBLY	846357	89536	846357	1	
A 5	✓ PROBE ASSEMBLY	773911	89536	773911	1	
A 6	✓ CLOCK MODULE ASSEMBLY	768812	89536	768812	1	
A 11	✓ I/O CONNECTOR PCA	767996	89536	767996	1	
A 24	✓ MULTI-FUNCTION INTERFACE II PCA	877808	89536	877808	1	
A 25	✓ PROBE I/O-ECL PCA	877811	89536	877811	1	
A 101	PWR SUP,150W,+5V,(2)+12V,-5V	772988	61852	XL160-3416	1	
A 102	DISK DRIVE,FLOPPY,3.5IN.,32MM BEZEL	880315	OJTT6	MP-F17W-50LW/32MM BEZEL	1	1
A 104	DISK DRIVE,RIGID,3.5IN.,40MB,SCSI	879903	OKAW4	CP-3040	1	2
A 106	MODULE,1024KX9 DRAM,80NS	830554	04713	MCM91000S-8	4	
DS 1	LED,RED,PCB MNT,LUM INT=0.5MCD	369777	28480	HLMP-1000	1	
E 1	TERM,FASTOM,REC,.187,18-22 AWG,INSUL	655001	00779	2-520194-2	1	
F 1	FUSE,5X20MM,0.125A,250V,FAST	573733	71400	GMA1-8	1	
F 2, 4	FUSE,.25X1.25,0.25A,250V,FAST	109314	71400	AGC1-4	2	
F 3, 5	FUSE,5X20MM,0.25A,250V,FAST	543504	71400	GMA1-4	2	
F 6	FUSE,.25X1.25,2A,250V,SLOW	109181	71400	MDL-2	1	
F 7	FUSE,5X20MM,1A,250V,SLOW	808055	61935	034.3117	1	
H 3	SCREW,PH,P,SEMS,STL,4-40,.250	185918		COMMERCIAL	2	
H 1	SCREW,PH,P,SS,4-40,.500	558825		COMMERCIAL	4	
H 4	SCREW,PH,P,STL,LOCK,6-32,.250	152140	73734	19042	35	3
H 5	NUT,WELD TAB,FLOATING,STL,10-32	743393	73020	P2F-10-S-ZC-CLEAR	2	
H 6	SCREW,PH,P,SS,10-32,.750	559187		COMMERCIAL	2	
H 7	SCREW,PH,P,STL,LOCK,8-32,.375	114124	89536	114124	6	
H 8	CONN ACC,D-SUB,LATCH BLOCK,SHORT,SLOT	811653	00779	745245-3	12	
H 9	SCREW,FIH,SL,STL,4-40,.375	129916		COMMERCIAL	4	
H 10	CONN ACC,D-SUB,SLIDING LOCK,POST ASSY	353201	54492	D53018	2	
H 11	SCREW,FIH,SL,STL,4-40,.250	810234		COMMERCIAL	8	
H 12	CONN ACC,D-SUB,JACK SCREW,4-40	448092	08718	D-20418-2	4	
H 13	RIVET,PUSH,UNIV,NYL,.16,.32	799957	06915	SR-4080	4	
H 14	SCREW,PH,P,STL,LOCK,6-32,.375	152165	73734	19044	2	
H 15	NUT,EXT LOCK,STL,6-32,.344OD	152819	78189	501-060800-00	2	
H 16	DUST FILTER, SET	773994	2K262	773994	1	
H 17	WASHER,SHLDR,NYL,.141,.320,.065	733345	9W423	2703-18265-N141	4	
H 18	RIVET,POP,DOME,AL,.125X.440	800763	OCLN7	AD44AH	4	
H 19	SCREW,PH,P,SEMS,STL,6-32,.375	177022		COMMERCIAL	4	
H 20	SCREW,PH,S,STL,M3X12	799502	19451	85-M3X12	4	4
H 21	SCREW,PH,P,STL,LOCK,6-32,.500	152173	73734	19046	4	2
H 22	SCREW, SHOULDER	775999	89536	775999	2	
H 23	CONN ACC,D-SUB,DUST CAP,37 SCKT	615138	89536	615138	4	
H 24	CONN ACC,D-SUB,DUST CAP,25 PIN	816371	89536	816371	2	
H 25	SCREW,PH,P,STL,LOCK,4-40,.250	129890	89536	129890	1	
H 26	CONN ACC,MICRO-RIBBON,SCREW LOCK KIT	836585	00779	554808-1	1	
J 1	CONN,COAX,BNC(F),PANEL	152033	74868	30355-1	1	
MP 1	LABEL, COPYRIGHT – 91	884176	89536	884176	1	
MP 2	HLDR PART,FUSE,CAP,5X20MM	461020	61935	031.1663	3	
MP 3	HLDR PART,FUSE,CAP,l/4X1-1/4	460238	61935	031.1666	3	
MP 5	SPACER,.187 HEX,AL,4-40,.500	192872	9W423	8106-A-0440	1	
MP 6	SHIELD, CLOCK MODULE	755793	22670	755793	1	
MP 7	CASE, CLOCK MODULE	755827	89536	755827	1	
MP 8	COVER	755686	89536	755686	1	

Table 5-1. 9100FT Series Final Assembly (cont)

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
MP 9	CASE, CLOCK MODULE	755652	89536	755652	1	
MP 11	KEYPAD CASE TOP	765008	89536	765008	1	
MP 12	KEYTOP, SET	775858	OABX4	775858	1	
MP 13	KEYPAD, ELASTOMERIC	764910	OK392	764910	1	
MP 15	TORSION SPRING	784025	89536	784025	2	
MP 16	KEYPAD CASE BOTTOM	765016	89536	765016	1	
MP 17	SPRING DETENT	765032	89536	765032	2	
MP 18	NAMEPLATE	787275	22670	787275	1	
MP 19	FRONT PANEL, PAINTED	764894	89536	764894	1	
MP 20	DISPLAY WINDOW, SHIELD	784009	22670	784009	1	
MP 21	LENS, 9100FT	899609	89536	899609	1	5
MP 22	KEYPAD OPENING SHIELD	767889	89536	767889	1	
MP 23	HINGE/DETENT HOUSING	765024	89536	765024	2	
MP 24	MAINFRAME BASE	767848	89536	767848	1	
MP 25	I/O CONNECTOR PANEL	767863	89536	767863	1	
MP 26	DECALS CHASSIS CONNECTOR	803221	22670	803221	1	
MP 27	FOOT,VINYL,NYL.PUSH RIVET,0.787X0.236	801001	06915	FF-008-P4X7	4	
MP 28	CABLE TIE,FLAT RETAINER,ADHESIVE BACK	564625	28213	3484-1000	2	
MP 29	REAR PANEL	767855	89536	767855	1	
MP 31	HLDR PART,FUSE,BODY 1/4X1-1/4,5X20MM	460329	61935	031.1673	1	
MP 32	EXPANSION SLOT COVER	768010	89536	768010	1	
MP 33	VIDEO SLOT COVER	768655	89536	768655	1	
MP 35	CABLE TIE,MOUNT,ADHESIVE,0.19" WIDTH	565036	06383	ABM2S-AT-0	2	
MP 36	CABLE ACCESS,TIE,4.00L,.10W,.75 DIA	172080	06383	SST-1M	1	
MP 37	SLEEV,POLYOL,SHRINK,.750-.375ID,BLACK	226365	88690	AF	3	
MP 38	MAINFRAME TOP COVER	773986	4N072	773986	1	
MP 39	SHIELDS RFI	768028	89536	768028	1	6
MP 40	LOUVER	787846	89536	787846	1	7
MP 41	POWER SUPPLY SHIELD ASSEMBLY, PLATED	830398	89536	830398	1	
MP 42	CABLE TIE,3.62"L,0.091"W,5/8 DIA	381533	06383	PLT1M	1	
MP 43	STUD ACCESS,RECEIVER,STL,.187 DIA	783134	78553	C2694-156-4	2	
MP 44	HARD DISK AND FLOPPY HOUSING	802033	89536	802033	1	8
MP 45	MOUNT,VIBRATION,GROMMET	782623	1M331	G-411-1	8	
MP 46	SPACER,.195 RND,SHLDR,NYL,.142,.300	782631	1M331	T-306	8	
MP 47	NAMEPLATE, SERIAL -REAR PANEL-	472795	85480	472795	2	9
MP 48	9100A PROBE ACCESSORIES	788554	89536	788554	1	
MP 49	9100 DISK SET	899588	89536	899588	1	
MP 50	MFI SLOT ESD COVER	819680	89536	819680	1	
MP 51	SSA DOCUMENT FOLDER	857479	89536	857479	1	
MP 52	ENVELOPE, REGISTRATION & SURVEY	822833	89536	822833	1	
MP 53	REC.MEDIA,DISK,3.5",DSDD,BOX.OF 10	757229	1EX28	757229	1	
MP 54	CABLE CLAMP,8"L,1-3/4"DIA,#6 SCREW	565580	06383	SSC2S-S6	1	
MP 55	DECAL FLUKE/PHILIPS ALLIANCE-(LT PWT)	865654	89536	865654	1	
MP 56	DECAL CSA	525527	22670	525527	1	
MP 57	BINDER & CASE FOR OPTIONS	855523	89536	855523	1	
MP 58	BAG,STATIC SHIELDING,24X24	853507	89536	853507	1	
MP 59	CARTON, 9100A	809038	89536	809038	1	
MP 60	END CAP SET, 9100A	809046	89536	809046	1	
MP 61	TRAY/DIVIDERS, 9100A	809053	89536	809053	1	
MP 62	CARTON, PADDED DISK	809129	89536	809129	1	
MP 63	BOX,FIBERBRD,W/INSERT,8.00,6.00,2.00	707851	0DSN7	CPC400	2	
MP 64	FOAM INSERT,SHIPPING CONTAINER	870162	89536	870162	1	

Table 5-1. 9100FT Series Final Assembly (cont)

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
MP 65	RELEASE NOTES	899658	89536	899658	1	
MP 66	DECAL, IEEE/488	877766	89536	877766	1	
S 1	SWITCH,ROCKER,DPST	800649	62440	232KW20B2C	1	
S 2	SWITCH,ROTARY,LINE SEL.,DPDT,2 POS.	799551	61935	SWA003.4501	1	
TM 1	9100 GETTING STARTED MANUAL	899893	89536	899893	1	
TM 2	9100 AUTOMATED OPERATIONS MAN	899885	89536	899885	1	
TM 3	9100 TECHNICAL USER MAN	899901	89536	899901	1	
TM 4	9100A APPLICATIONS MANUAL	813840	89536	813840	1	
TM 5	SUPPLEMENTAL POD INFO FOR 9100A/9105A	822866	89536	822866	1	
TM 6	9100 IEEE QUICK REF CARD	899922	89536	899922	1	
TM 7	9100 TL/1 REFERENCE MAN	899906	89536	899906	1	
W 1	CABLE ASSEMBLY, HARD DISK TO MFI	787895	89536	787895	1	2
W 2	CABLE ASSEMBLY, MICRO-CLIP	809178	89536	809178	1	
W 3	CABLE ASSY, CLOCK MODULE	853072	89536	853072	1	
W 4	CABLE,KEYPAD INTERFACE	773861	89536	773861	1	
W 5	CABLE,DISPLAY INTERFACE	773853	89536	773853	1	
W 6, 7	CABLE, PROBE I/O INTERFACE	773432	89536	773432	2	
W 8	IEEE CABLE ASSEMBLY	870360	89536	870360	1	
W 9	CABLE ASSEMBLY, LINE FILTER	773424	89536	773424	1	
W 10	CABLE ASSEMBLY, LINE SELECT	773267	89536	773267	1	
W 11	CABLE ASSY, TURBO FAN	899740	89536	899740	1	
W 12, 21	CABLE ASSEMBLY, RS232 M	787838	89536	787838	2	
W 13	CABLE ASSEMBLY, BNC	801944	89536	801944	1	
W 15	WIRE,TEF,UL1180,18AWG,STRN,BLK	135814	89536	135814	1	
W 16	CABLE, A C POWER COMNECT	749903	89536	749903	1	
W 17	CABLE ASSEMBLY, D C HARNESS	773887	89536	773887	1	
W 18	CABLE,DISK DRIVE	773846	89536	773846	1	10
W 19	CABLE, DISK DRIVE POWER	884205	89536	884205	1	11
W 20	CORD,LINE,5-15/IEC,3-18AWG,SVT,5.5 FT	343723	70903	17237	1	

NOTES:

↙ Static sensitive part.
1. For 9105FT quantity is 2.
2. Not used an 9105FT.
3. For 9105FT quantity is 37.
4. For 9105FT quantity is 8.
5. For 9105FT, ordez steck no. 899612.
6. Por 9105FT, order stock no. 805713, quantity 2.
7. For 9105FT, order stock no. 787853.
8. For 9105FT, order stoek no. 788521.
9. For 9105FT quantity is 1.
10 . For 9105FT, order stock no. 788547.
11 . For 9105FT, order stock no. 805705.

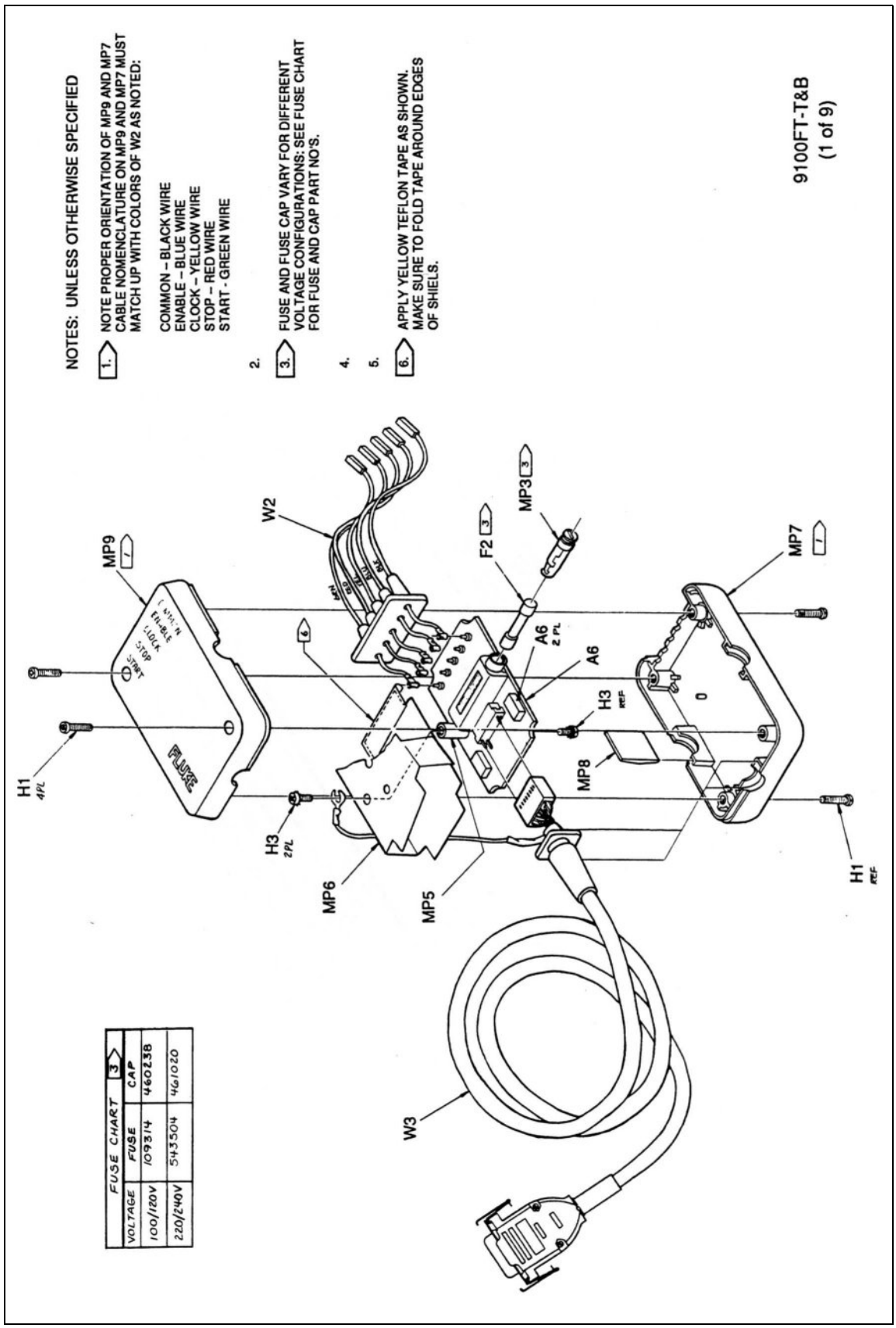


Figure 5-2. 9100FT Final Assembly

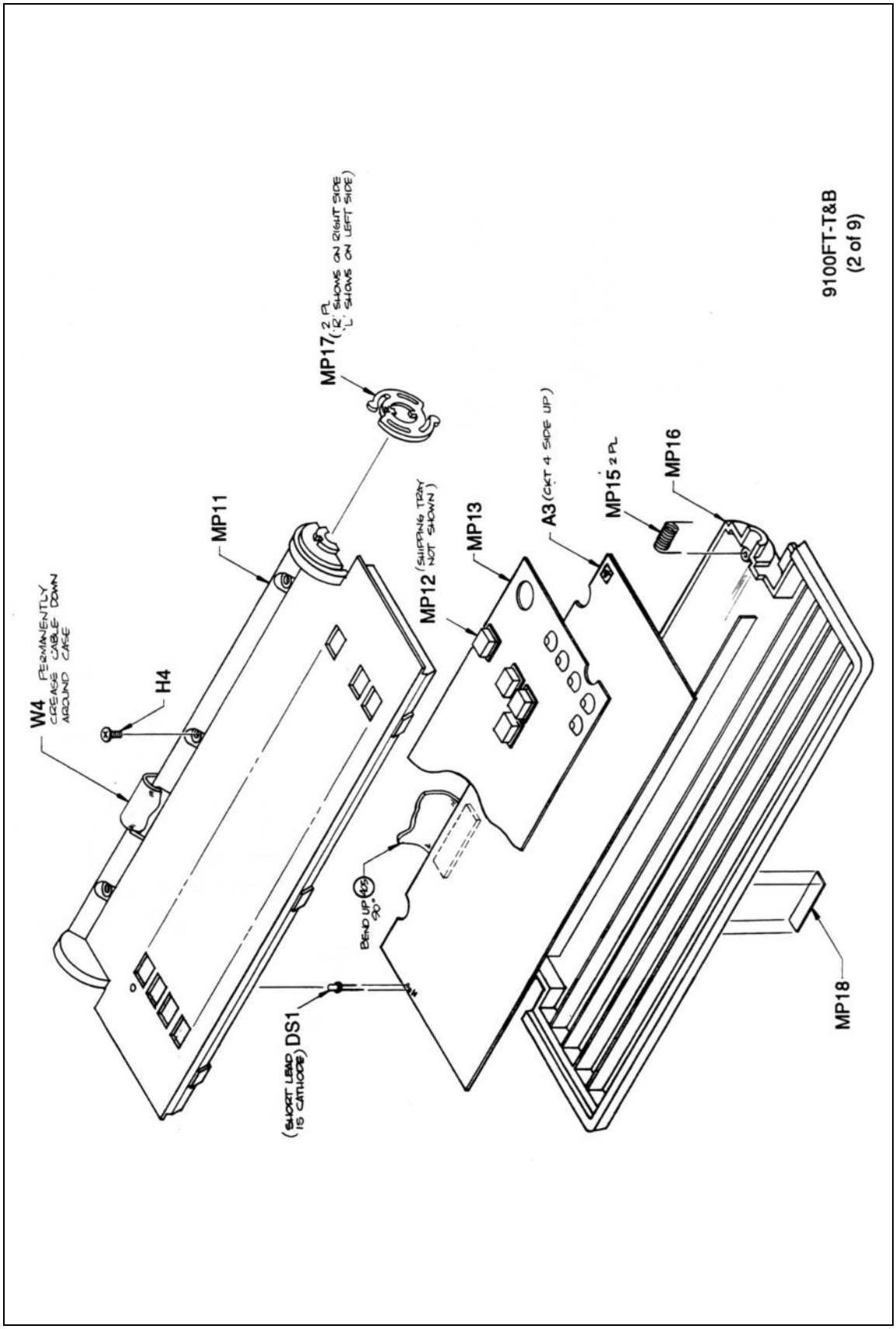


Figure 5-2. 9100FT Final Assembly (cont)

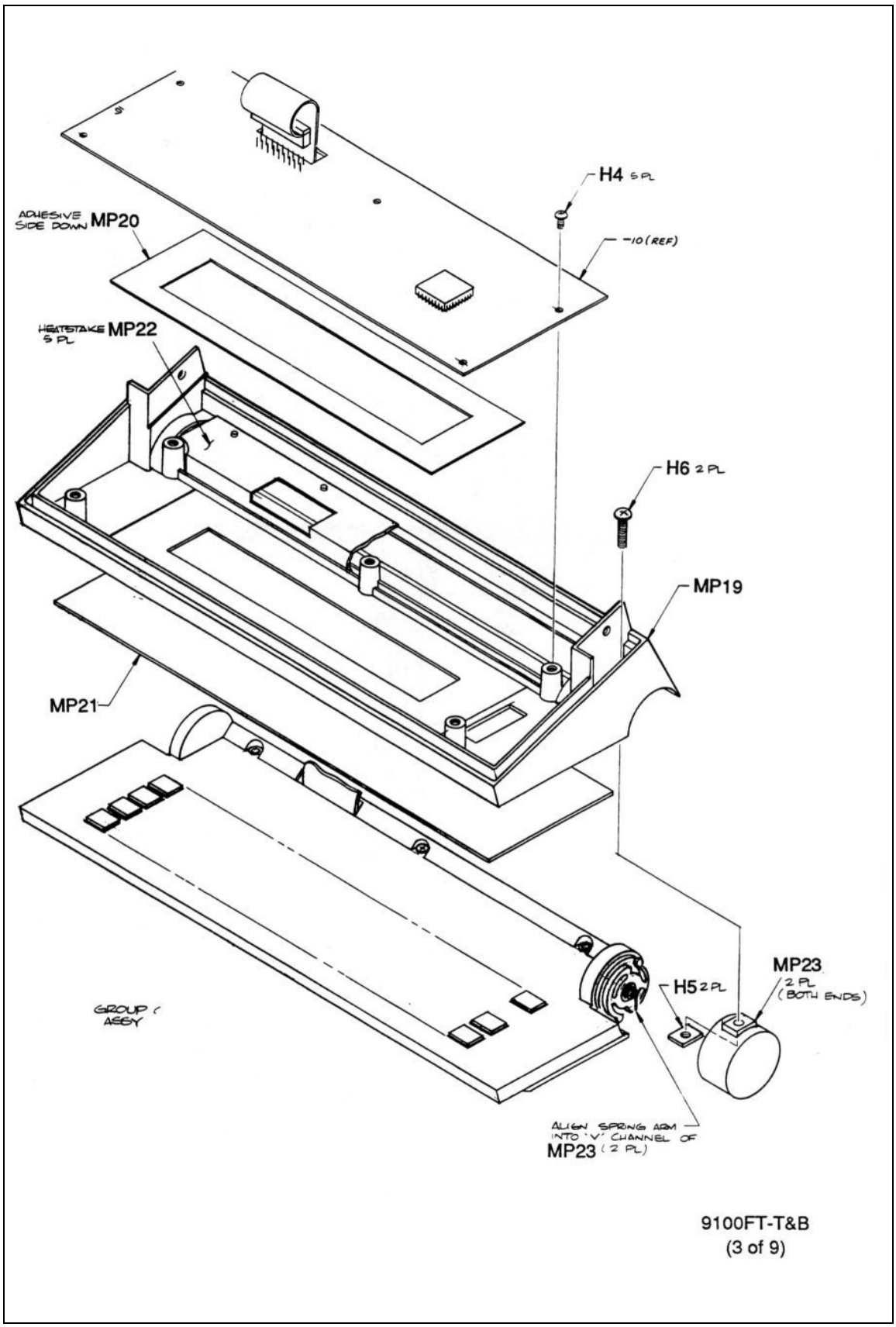


Figure 5-2. 9100FT Final Assembly (cont)

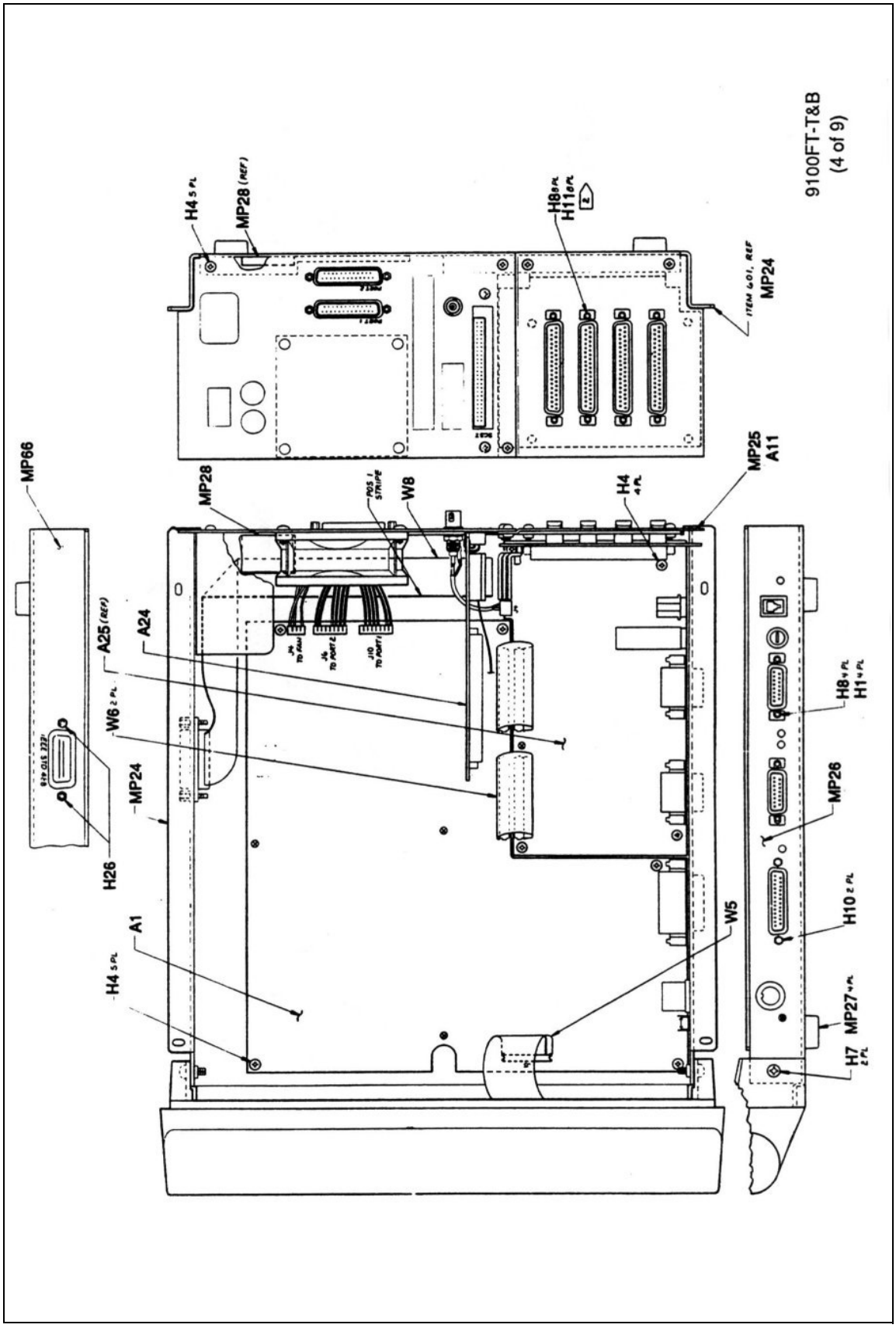


Figure 5-2. 9100FT Final Assembly (cont)

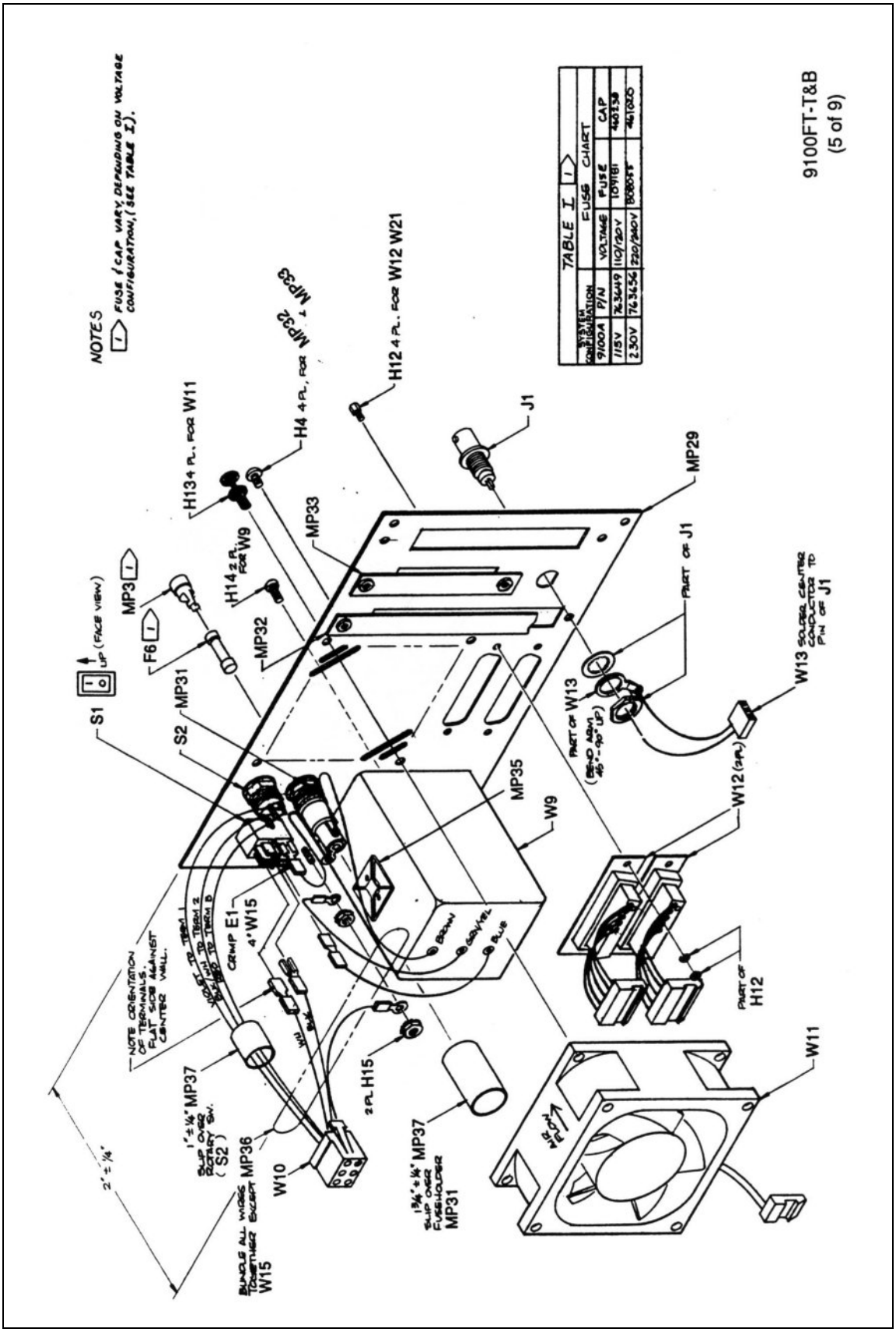


Figure 5-2. 9100FT Final Assembly (cont)

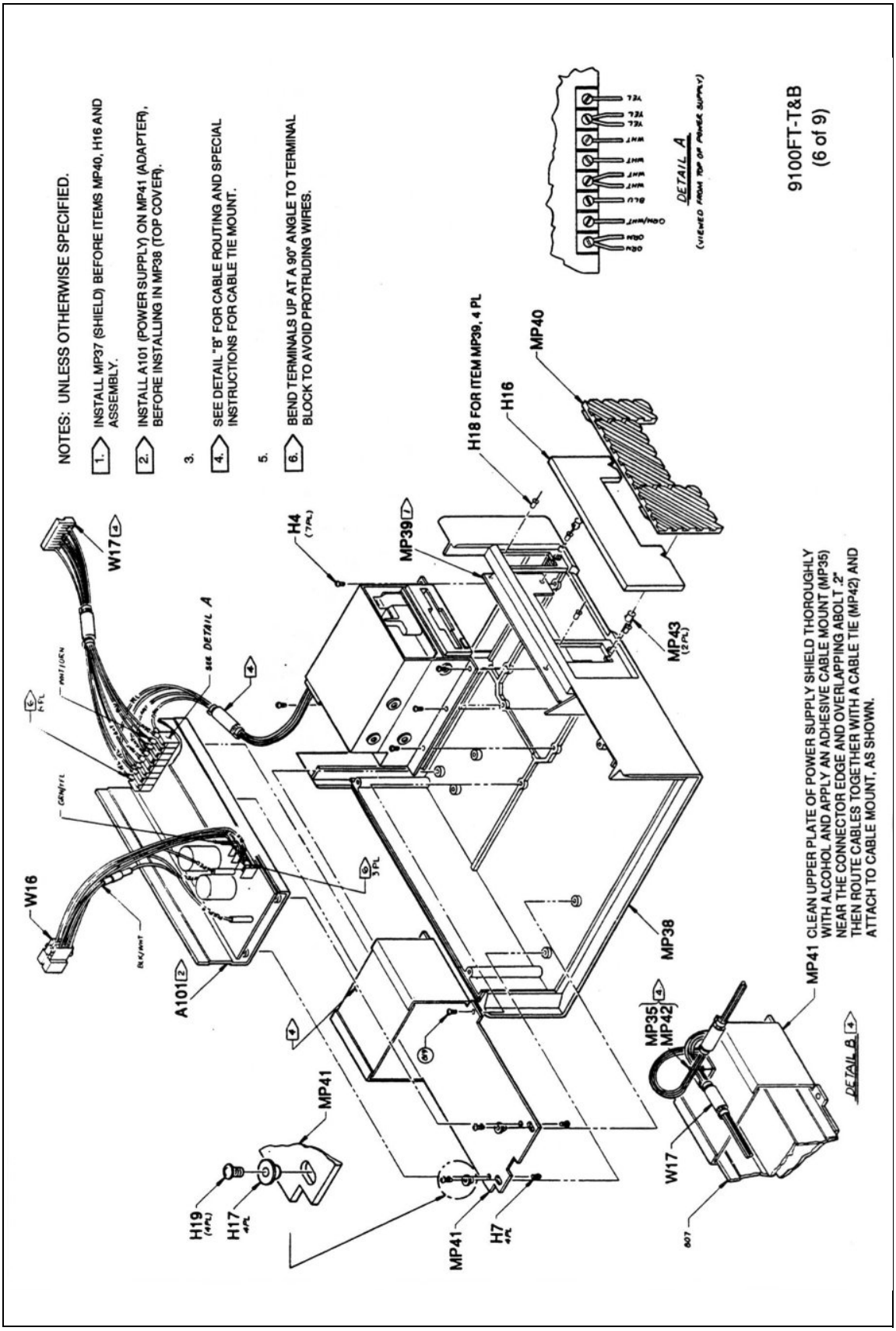


Figure 5-2. 9100FT Final Assembly (cont)

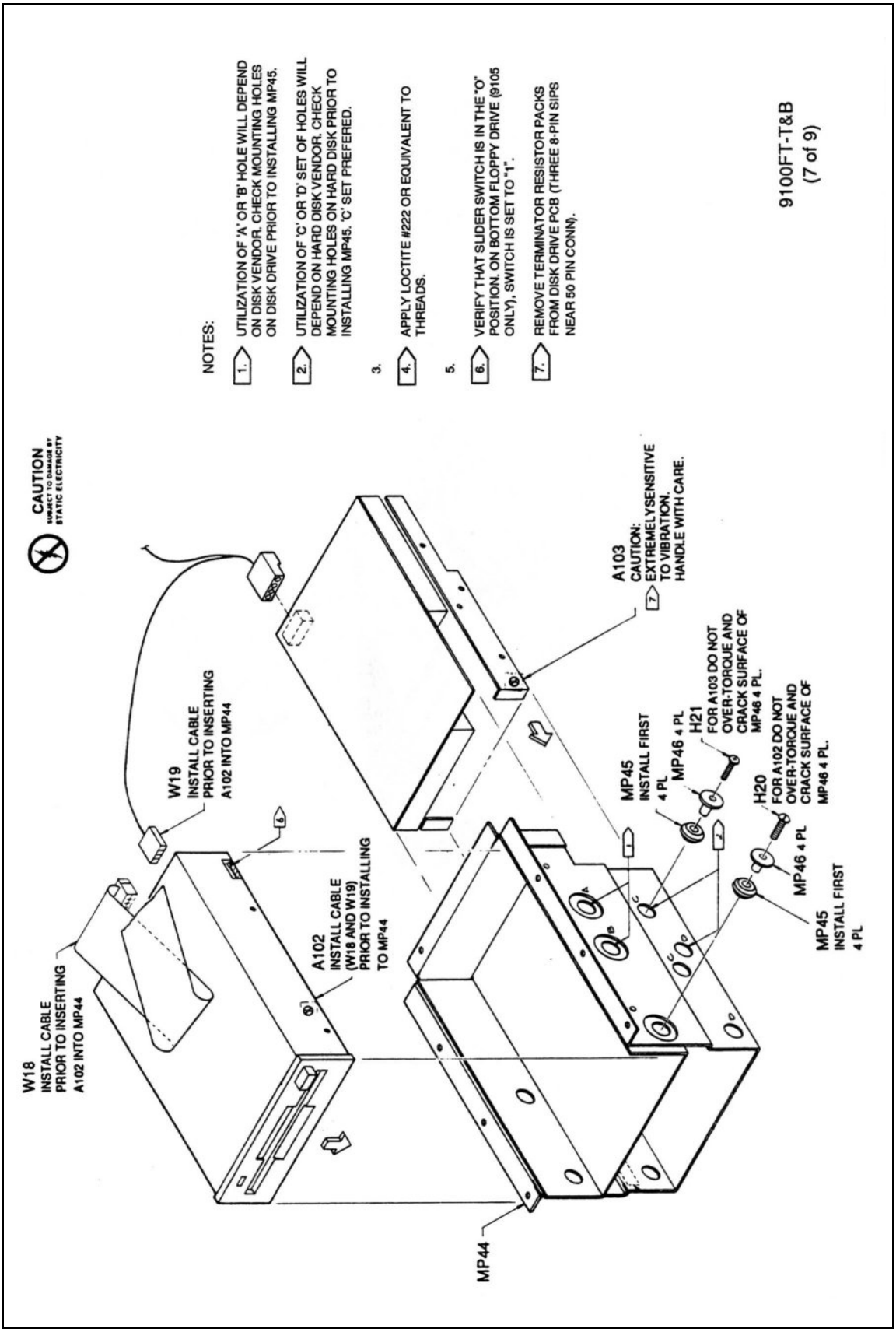


Figure 5-2. 9100FT Final Assembly (cont)

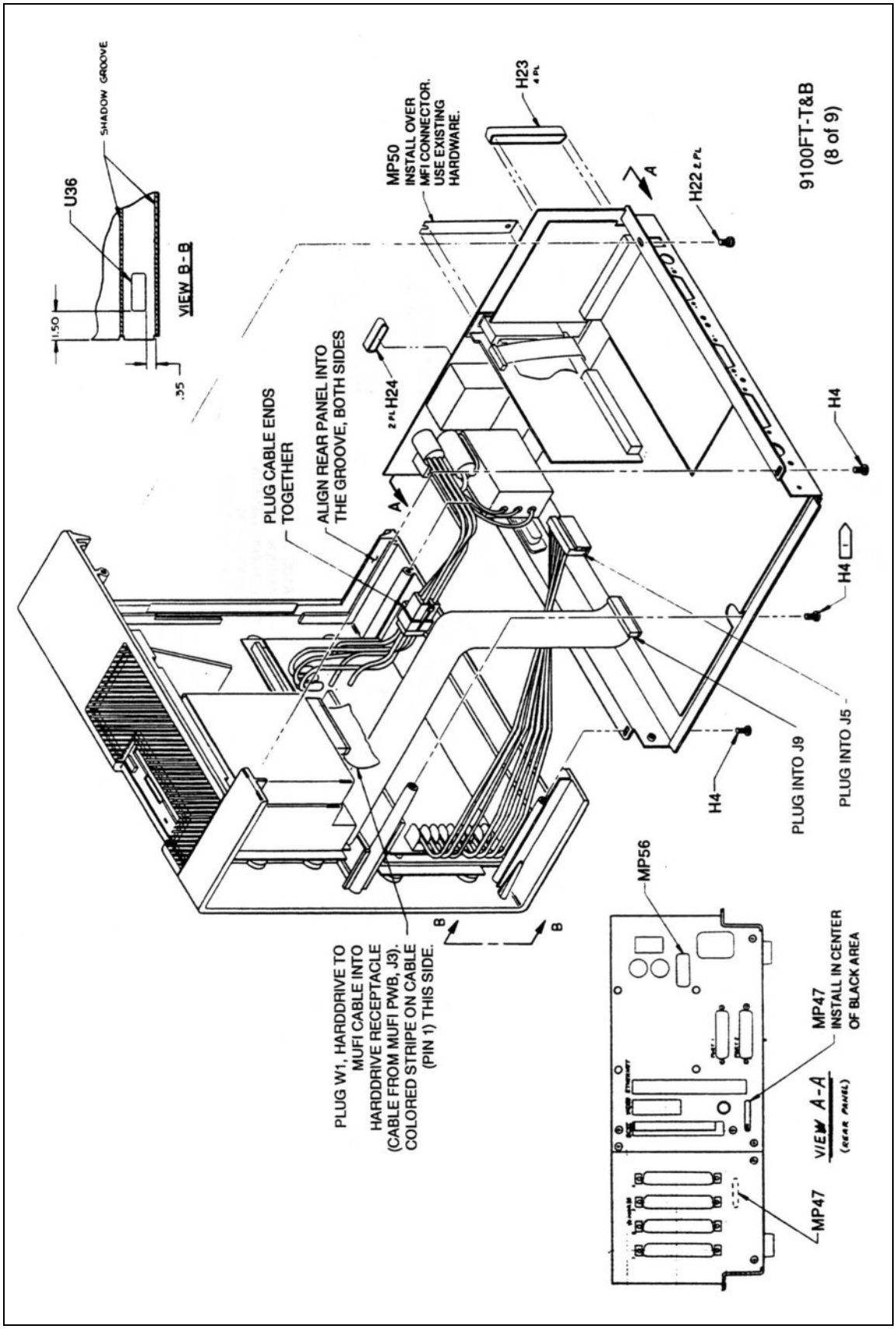


Figure 5-2. 9100FT Final Assembly (cont)

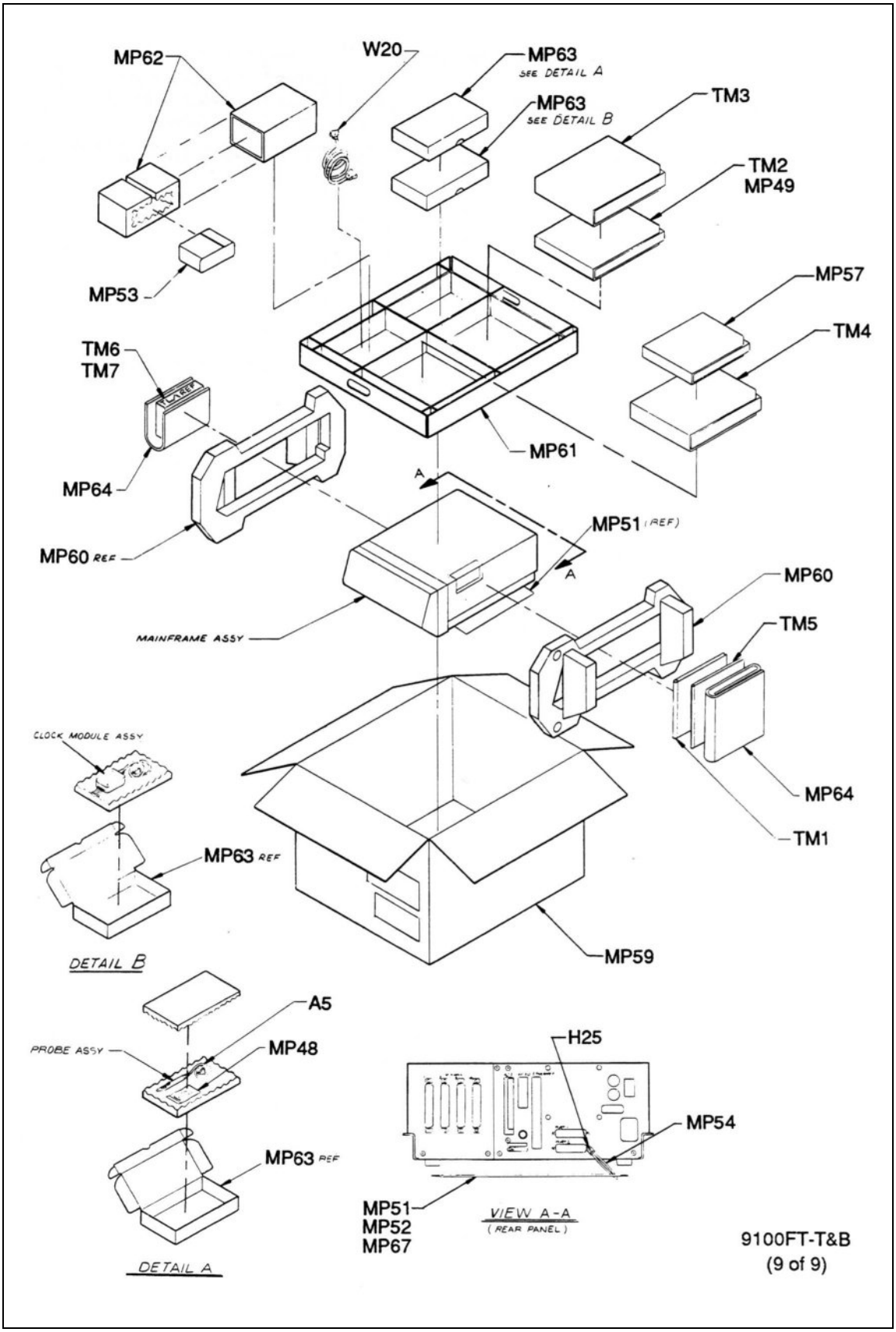


Figure 5-2. 9100FT Final Assembly (cont)

Table 5-2. A1 Main PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 1- 12, 16- C 21, 28- 31, C 33, 36- 38, C 41- 44, 46- C 49, 51, 52 C 54, 55, 59- C 75, 77- 88, C 90, 91	CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287 747287 747287 747287 747287 747287 747287 747287 747287	04222	12063C104KAT060B	96	
C 13-15, 24, C 34, 35, 45, C 50, 53, 56- C 58, 76,111, C 122-124	CAP,TA,10UF,+-20%,25V	772491 772491 772491 772491 772491	56289	195D106X0025G2B	17	
C 22, 23, 32, C 89	CAP,CER,0.01UF,+-20%,100V,X7R,1206	742981 742981	04222	12061C103MA1050B	4	
C 25, 26, 99, C 100	CAP,CER,47PF,+-10%,50V,COG,1206	747352 747352	04222	12065A470KAT060B	4	
C 27, 40	CAP,CER,10PF,+-10%,50V,COG,1206	747311	04222	12065A100KAT060B	2	
CR 1- 6	✓ DIODE,SI,BV=200V,IO=10A,DUAL,SOT89	742973	25088	BAW79C E6327	6	
CR 7, 8, 11	✓ DIODE,SI,BV=75.0V,IO=100MA,MLF	742064	8A233	BAS32	3	
CR 9, l0, 12	✓ DIODE,SI,SCHOTTKY,30V,1.1A,SOT89	782573	59993	10JQ030TRRM	3	
J 1	HEADER,2 ROW,.100CTR,34 PIN	643841	00779	5227-139-8	1	
J 2	HEADER,l ROW,.100CTR,2 PIN	602698	00779	640456-2	1	
J 3, 4	HEADER,2 ROW,.100CTR,40 PIN	603670	00779	2-102973-0	2	
J 5	HEADER,1 ROW,.156CTR,10 PIN	446724	00779	1-640388-0	1	
J 7	CONN,D-SUB,PWB,RT ANG,25 SCKT	782144	00779	747846-4	1	
J 8	HEADER,1 ROW,.100CTR,4 PIN	631184	00779	640456-4	1	
J 9	HEADER,2 ROW,.100CTR,34 PIN	658047	00779	1-102973-7	1	
J 10	HEADER,2 ROW,.100CTR,20 PIN	782185	00779	1-102973-0	1	
J 11, 13	CONN,DIN41612,TYPE R,96 PIN	747808	00779	532523-1	2	
J 12	CONN,DIN41612,TYPE R,64 PIN	782094	00779	532523-2	1	
J 14, 16	HEADER,1 ROW,.l00CTR,8 PIN	520502	22526	65502-408	2	
J 15	CONN,CIRC,DIN,RT ANG,PWB,5 PIN @ 180	772178	00779	211450-1	1	
L 1- 5	CHOKE	502138	89536	502138	5	
MP 1	SPACER, LED .250 LG	426882	89536	426882	2	
MP 2	HOLDER,FUSE,5X20MM,PCB	772475	75915	111501	2	
MP 3	SPACER,.440 RND,SOLUBLE,.065SLOT,.150	334797	32559	TO-35-15-E	5	
MP 4	LABEL,ADHES,MYLAR,BAR CODE,1.25,.245	807099	9R216	807099	1	
Q 1, 2	✓ TRANSISTOR,SI,N-MOS,1W,4 PIN DIP	800391	17856	V11974	2	
Q 3	✓ TRANSISTOR,SI,NPN,SMALL SIGNAL,SOT-23	742031	73445	BCX19TRL	1	
R 1, 6, 26, R 28, 29, 36- R 40, 84- 86, R 88	RES,CERM,33,+-5%,.125W,200PPM,1206	746248 746248 746248 746248	91637	CRCW1206-33ROJB02	14	
R 2, 4, 7, R 9, 80	RES,CERM,39K,+-5%,.125W,200PPM,1206	746677 746677	91637	CRCW1206-3902JB02	5	
R 3, 8, 79	RES,CERM,3K,+-5%,.125W,200PPM,1206	746511	91637	CRCW1206-3001JB02	3	
R 5, 10, 23, R 24, 77	RES,CERM,750,+-5%,.125W, 200PPM,1206	746404 746404	91637	CRCW1206-7500JB02	5	
R 11, 13	RES,CERM,390,+-5%,.125W,200PPM,1206	740498	91637	CRCW1206-3900JB02	2	
R 12, 14, 22, R 25, 27, 35, R 41, 43, 48, R 54, 56, 59, R 62, 65, 76, R 81- 83, 87, R 96, 99-104, R 108-112,116, R 117,119	RES,CERM,l0K,+-5%,.125W,200PPM,1206	746610 746610 746610 746610 746610 746610 746610 746610 746610	91637	CRCW1206-1002JB02	34	
R 15, 17, 57, R 91,106,107, R 113-115,118	RES,CERM,4.7K,+-5%,.125W,200PPM,1206	740522 740522 740522 740522	91637	CRCW1206-4701JB02	10	
R 16, 18	RES,CERM,220,+-5%,.125%,200PPM,1206	746347	91637	CRCW1206-2200JB02	2	

Table 5-2. A1 Main PCA (cont)

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
R 19, 20	RES,CERM,510K,+-5%,.125W,200PPM,1206	746800	91637	CRCW1206-5103JB02	2	
R 21, 78	RES,CERM,100K,+-5%,.125W,200PPM,1206	740548	91637	CRCW1206-1003JB02	2	
R 30- 33, 42,	RES,CERM,1.2K,+-5%,.125W,200PPM,1206	746412	91637	CRCW1206-1202JB02	16	
R 53, 55, 63,		746412				
R 89, 90, 92-		746412				
R 95, 97, 98		746412				
R 34	RES,CERM,2.2K,+-5%,.125W,200PPM,1206	746479	91637	CRCW1206-2201JB02	1	
R 44- 47, 49,	RES,CERM,51,+-5%,.125W,200PPM,1206	746271	91637	CRCW1206-51R0JB02	6	
R 50		746271				
R 64	RES,CERM,5.1K,+-5%,.125W,200PPM,1206	746560	91637	CRCW1206-5101JB02	1	
RN 1, 2	RES,CERM,SIP,10 PIN,9 RES,l0K,+-2%	414003	91637	CSC10A-01-103G	2	
S 1	SWITCH,DIP,SPST,PIANO,SEALED,8 POS	658567	00779	1-435802-5	1	
S 2	SWITCH,PUSHBUTTON,SPST,MOMENTARY	782433	61964	B3F-3122	1	
T 1	TRANSFORMER,CONVERTER	775932	89536	775932	1	
TM 1	THERMISTOR,DISC,NEG,100K,+-5%,25C	877035	89536	877035	1	
TP 1, 5, 6,	TERM,UNINSUL,WIRE FORM,TEST POINT	781237	27918	TP102-01	6	
TP 9- 11		781237				
U 1, 3	✗ IC,BIPOLAR,QUAD RS-232 RECEIVER,SOIC	867812	01295	SN75154DR	2	
U 2, 4	✗ IC,BIPOLAR,DUAL RS-232 DRIVER,SOIC	742403	01295	SN75150DR	2	
U 5, 6	✗ ISOLATOR,OPTO,HI-SPEED,DUAL	429894	28480	HCPL-2531	2	
U 7, 12	✗ IC,NMOS,DUAL ASYN RECVR/TRANS,PLCC	742999	18324	SCN2681AC1A44T	2	
U 8	✗ IC,NMOS,16X16 BIT NOVRAM	781187	60395	781187	1	
U 9	✗ IC,CMOS,QUAD 2 INPOUT NAND GATE,SOIC	838177	07263	74ACT00SCT	1	
U 10	✗ IC,TTL,HEX BUFFER W/OPEN COLL,SOIC	742387	01295	SN7417DR	1	
U 11	✗ IC,CMOS,HEX INVERTER,SOIC	742585	18324	N74HCT040	1	
U 13, 28	✗ IC,ALSTTL,OCTAL LINE DRVR,SOIC	741744	01295	SN74ALS244ADWR	2	
U 14	✗ IC,CMOS,8 BIT P/S-IN,S-OUT SHFT,SOIC	782904	18324	74HCT165DT	1	
U 15	✗ IC,LSTTL,OCTAL BUFFER INVERTED,SOIC	742627	01295	SN74LS240DR	1	
U 16	✗ IC,CMOS,FLOPPY INT CKT,PLCC	851316	53848	FDC92C39BTTRLJP	1	
U 17	✗ IC,NMOS,FLOPPY DISK FORMTR CNTLR,PLCC	782870	53848	FDC1797-02LJP	1	
U 18	✗ IC,ALSTTL,QUAD 2 INPUT NOR GATE,SOIC	782284	01295	SN74ALS02DR	1	
U 19	✗ IC,ALSTTL,3-8 LINE DCDR W/ENABLE,SOIC	741686	01295	SN74ALS138DR	1	
U 20, 39	✗ IC,CMOS,DUAL D F/F,+EDG TRG,SOIC	837930	12040	74ACT74SCT	2	
U 21	OSCILLATOR,32MHZ,TTL CLOCK	742338	01537	K1100AM32	1	
U 22, 33	✗ IC,CMOS,OCTAL BUS TRANSCEIVER,SOIC	742577	01295	SN74HCT245DWR	2	
U 23	✗ IC,PROG GATE ARRAY,2000 G,70 MHZ,PLCC	887133	68994	XC3020-70PC84C	1	
U 24	✗ IC,DYNAMIC RAM CONTROLLER,25 MHZ,PLCC	887158	44648	KS84C32-25CL	1	
U 25	✗ IC,PROG GATE ARRAY,3000 G,70 MHZ,PQFP	887138	68994	XC3030-70PQ100C	1	
U 26	✗ PROGRAMMED EPROM, TURBO	899679	89536	899679	1	
U 27	✗ IC,CMOS,OCTAL D F/F,+EDG TRG,SOIC	799577	01295	SN74HCT374DWR	1	
U 29	✗ IC,FTTL,QUAD BUS BUFFER,SOIC	801324	18324	74F125DT	1	
U 30, 47	✗ IC,CMOS,HEX INVERTER W/SCHT TRIG,SOIC	876813	04713	MC74ACT14DR1	2	
U 31	✗ PROGRAMMED GAL16V8, TURBO	899682	89536	899682	1	
U 32	✗ PROGRAMMED GAL20V8, TURBO	899687	89536	899687	1	
U 34	✗ IC,COMPARATOR,QUAD,14 PIN,SOIC	741561	18324	LN339DT	1	
U 35, 37, 48	✗ MODULE,1024KX9 DRAM,80NS	830554	04713	MCM91000S-10	4	
U 51	✗	830554				
U 36	✗ PROGRAMMED XC1765, TURBO	915673	89536	915673	1	
U 40	✗ IC,MPU,ENHANCED,32 BIT,25 MHZ,QFP	887153	04713	MC68030FE25 [X]	1	
U 41, 42	✗ IC,CMOS,16 BIT BUS TRNSCVR/REG,SOIC	887141	01295	74ACT16646DLR	2	
U 44	OSCILLATOR,50MNHZ,TTL CLOCK	887146	91637	XO-43D50	1	
U 49	✗ IC,MICROMONITOR,WATCHDOG TIMER,SOIC	876990	OBOA9	DS1232S-TRL	1	
U 53	✗ IC,ALSTTL,QUAD 2 INPUT AND GATE,SOIC	741827	01295	SN74ALSO8DR	1	
U 54	✗ IC,ALSTTL,QUAD 2 INPUT OR GATE,SOIC	742460	01295	SN74ALS32DR	1	
XU 26	SOCKET,IC,32 PIN	807156	00779	2-644018-3	1	

Table 5-2. A1 Main PCA (cont)

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
XU 35, 37, 38, XU 43, 48, 50- XU 52	CONN,PWB EDGE,REC,.100CTR,30 POS	806828 806828 806828	00779	821828-2	8	
XU 36	SOCKET,IC,8 PIN	478016	00779	2-640463-1	1	
Y 1	CRYSTAL,3.6864MHZ,+-5OPPM,HC-49SG	875625	61429	FOX-HC49SG-3.6864MHZ	1	
NOTES:	↯ Static sensitive part.					

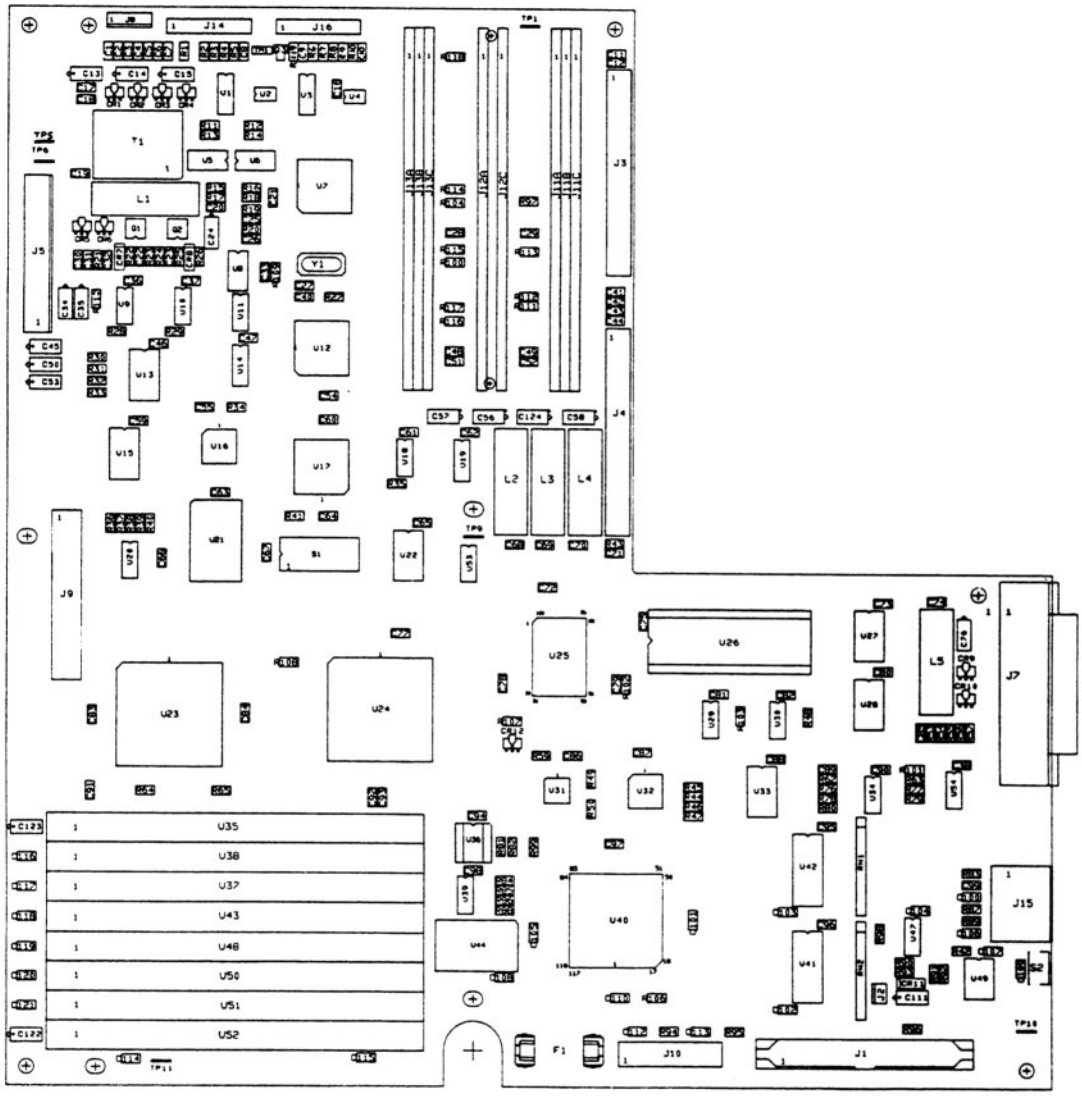


Figure 5-3. A1 Main PCA

Table 5-3. A2 Display Interface PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C l, 8	CAP,CER,5.6PF,+-10%,50V,COG,1206	782409	04222	12065A5R6KAT050B	2	
C 2	CAP,TA,1.5UF,+-20%,50V	780478	56289	195D155X0050F2B	1	
C 3, 4	CAP,TA,10UF,+-20%,25V	772491	56289	195D106X0025G2B	2	
C 5, 70- 78,	CAP,CER,0.01UF,+-20%,100V,X7R,1206	742981	04222	12061C103MA1050B	41	
C 101-131		742981				
C 6, 7	CAP,CER,0.1UF,+-l0%,25V,X7R,1206	747287	04222	12063C104KAT060B	2	
CR 1- 7	LED,RED,RECTANGLE,PCB MOUNT	504761	58361	MV57124A	7	
E 1	AF TRANSD,PIEZO,24 MM	602490	51406	PKM24-4A1	1	
J 1, 2	HEADER,2 ROW,.100CTR,20 PIN	782185	00779	1-102973-0	2	
MP 1	LABEL,ADHES,MYLAR,BAR CODE,1.25,.245	807099	9R216	807099	1	
MP 2	DISPLAY ALIGNMENT FIXTURE	788570	89536	788570	1	
Q 1- 4	✓ TRANSISTOR,SI,PNP,SMALL SIGNAL,SOT-23	742023	73445	BCX17TRL	4	
Q 5- 8	✓ TRANSISTOR,SI,NPN,SMALL SIGNAL,SOT-23	742031	73445	BCX19TRL	4	
R 1- 4, 6-	RES,CERM,1.1K,+-5%,.125W,200PPM,1206	746008	91637	CRCW1206-1101JB02	16	
R 13, 15, 16,		746008				
R 48, 49		746008				
R 5	RES,CERM,100K,+-5%,.125W,200PPM,1206	740548	91637	CRCW1206-1003JB02	1	
R 14, 17	RES,CERM,6.8K,+-5%,.125W,200PPM,1206	746024	91637	CRCW1206-6801JB02	2	
R 18, 19	RES,CERM,620,+-5%,.125W,200PPM,1206	745984	91637	CRCW1206-6200JB02	2	
R 20	RES,CERM,330,+-5%,.125W,200PPM,1206	746370	91637	CRCW1206-3300JB02	1	
R 21	RES,CERM,470,+-5%,.125W,200PPM,1206	740506	91637	CRCW1206-4700JB02	1	
R 22- 29	RES,CERM,10K,+-5%,.125W,200PPM,1206	746610	91637	CRCW1206-1002JB02	8	
R 30, 31	RES,CERM,6.2K,+-5%,.125W,200PPM,1206	746016	91637	CRCW1206-6201JB02	2	
R 32, 42- 47	RES,CERM,180,+-5%,.125W,200PPM,1206	746321	91637	CRCW1206-1800JB02	7	
R 33, 34, 41,	RES,CERM,4.7K,+-5%,.125W,200PPM,1206	740522	91637	CRCW1206-4701JB02	4	
R 50		740522				
R 35, 36	RES,CERM,100,+-5%,.125W,200PPM,1206	746297	91637	CRCW1206-1000JB02	2	
R 37	RES,CERM,3K,+-5%,.125W,200PPM,1206	746511	91637	CRCW1206-3001JB02	1	
R 38	RES,CERM,7.5K,+-5%,.125W,200PPM,1206	746586	91637	CRCW1206-7501JB02	1	
R 39	RES,CERM,2K,+-5%,.125W,200PPM,1206	746461	91637	CRCW1206-2001JB02	1	
R 40	RES,CERM,1.8K,+-5%,.125W,200PPM,1206	746453	91637	CRCW1206-1801JB02	1	
TP 1- 7	TERM,UNINSUL,WIRE FORM,TEST POINT	781237	27918	TP102-01	7	
U 1	✓ IC,NMOS,8 BIT MPU,9100A-90220	855148	56708	Z8611PS	1	
U 2	✓ IC,LSTTL,OCTAL D F/F,+EDG TRG,SOIC	741975	18324	N74LS374DT	1	
U 3	✓ IC,2K X 8 STATIC RAM,120NSEC,SOIC	742783	65786	CY7C128-55SC	1	
U 4	✓ IC,LSTTL,DUAL DIV BY 2, 5 CNTR,SOIC	741967	18324	N74LS390DT	1	
U 5- 12	✓ IC,BIMOS,DISPLAY DRIVER,80V,PLCC	741231	56289	5818EPF-1	8	
U 13, 14	✓ IC,LSTTL,DUAL D F/F,+EDG TRG,SOIC	740985	18324	N74LS74ADT	2	
U 15, 27	✓ IC,ALSTTL,DUAL JK F/F,-EDG TRG,SOIC	807578	01295	SN74ALS112ADR	2	
U 16	✓ IC,LSTTL,QUAD 2 INPUT NAND GATE,SOIC	741033	18324	N74LS00DT	1	
U 17, 31	✓ IC,LSTTL,QUAD 2 INPUT NOR GATE,SOIC	741025	18324	N74LS02DT	2	
U 18	✓ IC,CMOS,HEX INVERTER,SOIC	742585	18324	N74HCT040	1	
U 19, 20	✓ IC,LSTTL,TRIPLE 3-INPUT AND GATE,SOIC	741264	18324	N74LS10D	2	
U 21	✓ IC,LSTTL,QUAD 2 INPUT OR GATE,SOIC	740878	18324	N74LS32D	1	
U 22	✓ IC,TTL,HEX INVERTER,W/OPEN COLL,SOIC	741249	18324	N7406DT	1	
U 23, 24	✓ IC,CMOS,8 BIT P/S-IN,S-OUT SHFT,SOIC	782904	18324	74HCT165DT	2	
U 25, 30	✓ IC,ALSTTL,OCTL D F/F,+EDG TRG,SOIC	741769	01295	SN74ALS273DWR	2	
U 26	✓ IC,LSTTL,BCD-DEC,DECODER/DRIVER,SOIC	742007	01295	SN74LS145DR	1	
U 28	✓ IC,LSTTL,DIV BY 16 BINARY COUNTR,SOIC	741991	18324	N74LS163ADT	1	
U 29	✓ IC,BPLR,DUAL TIMER,SOIC	741959	18324	NE556DT	1	
VF 1	TUBE,DISPLAY,VAC FLUOR, PATTERN DIS	742056	0BW21	DM256X26G	1	
VR 1, 2	✓ ZENER,UNCOMP,3.3V,5%,76MA,lW,MLF	800599	01537	MLL4728AT1	2	
XU 1	SOCKET,IC,40 PIN	429282	00779	2-640379-1	1	
Y 1	CRYSTAL,9.8304MHZ,+-50PPM,HC-49SG	867028	61429	FOX-HC49SG-9.8304MHZ	1	
NOTES:	✓ Static sensitive part.					

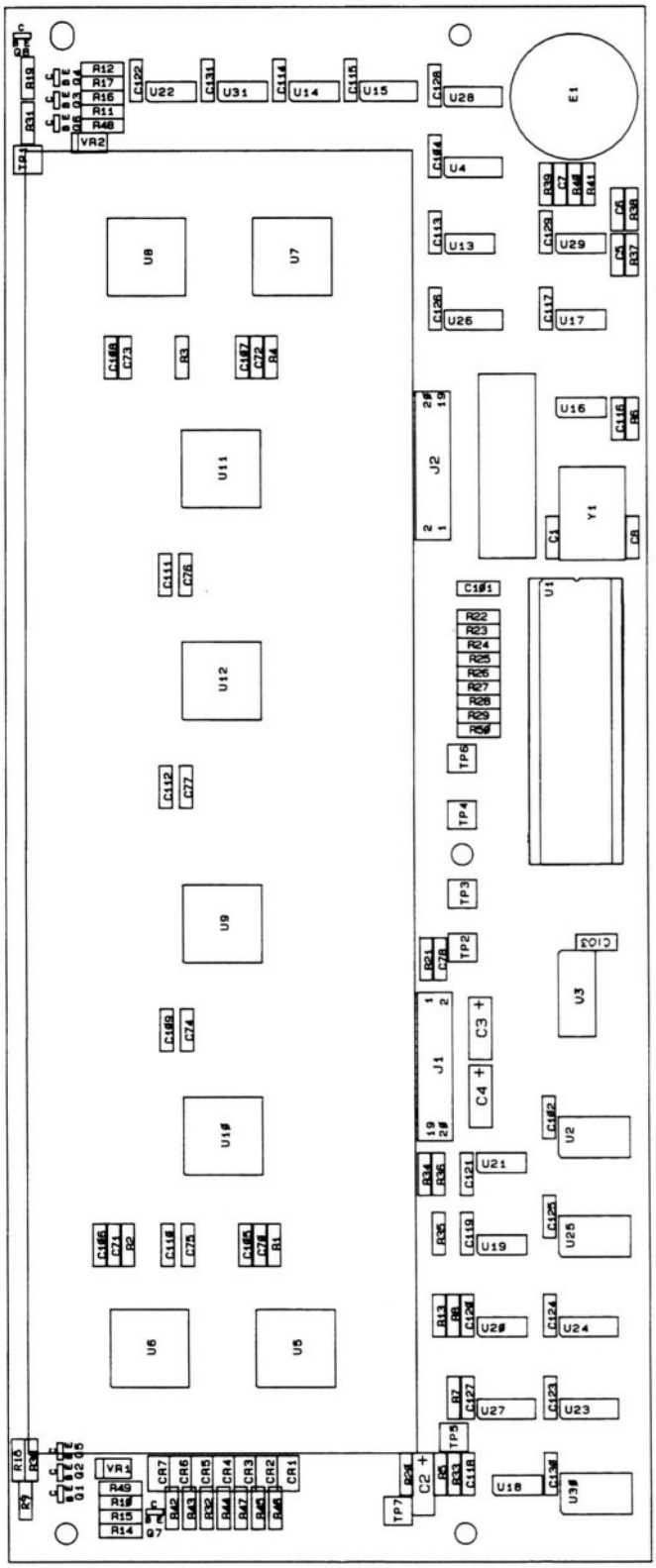


Figure 5-4. A2 Display Interface PCA

Table 5-4. A4 Video Controller PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 1,101-131	CAP,CER,0.01UF,+-10%,50V,X7R,1206	747261	04222	12065C103KAT060R	32	
C 2, 8	CAP,CER,O.1UF,+-10%,25V,X7R,1206	747287	04222	12063C104KAT060B	2	
C 3, 7	CAP,TA,10UF,+-20%,25V	772491	56289	195D106X0025G2B	2	
C 4- 6	CAP,CER,33PF,+-10%,50V,COG,1206	769240	04222	12065A330KAT050B	3	
C 9, 10	CAP,CER,120PF,+-10%,50V,COG,1206	740589	04222	12065A121KAT060B	2	
H 1	SCREW,THD CUT,PH,P,SS,4-24,.375	183574		COMMERCIAL	2	
H 2	LABEL,ADHES,MYLAR,BAR CODE,l.25,.245	807099	9R216	807099	1	
J 1	CONN,DIN41612,TYPE R,RT ANG,64 SCKT	782102	00779	531796-2	1	
J 2	CONN,D-SUB,PWB,RT ANG,9 SCKT	782789	00779	205866-1	1	
Q 1	✓ TRANSISTOR,SI,NPN,SMALL SIGNAL,SOT-23	742676	04713	MMBT3904T	1	
Q 2	✓ TRANSISTOR,SI,PNP,SMALL SIGNAL,SOT-23	742684	04713	MMBT3906T	1	
R 1- 5, 14,	RES,CERM,330,+-5%,.125W,200PPM,1206	746370	91637	CRCW1206-3300JB02	7	
R 15		746370				
R 6, 13	RES,CERM,510,+-5%,.125W,200PPM,1206	746388	91637	CRCW1206-5100JB02	2	
R 7- 11	RES,CERM,158,+-1%,.125W,100PPM,1206	769828	89536	769828	5	
R 12	RES,CERM,1K,+-5%,.125W,200PPM,1206	745992	91637	CRCW1206-1001JB02	1	
R 16	RES,CERM,470,+-5%,.125W,200PPM,1206	740506	91637	CRCW1206-4700JB02	1	
R 17	RES,CERM,47,+-5%,.125W,200PPM,1206	746263	91637	CRCW1206-47ROJB02	1	
R 18	RES,CERM,220,+-5%,.125W,200PPM,1206	746347	91637	CRCW1206-2200JB02	1	
R 19	RES,CERM,2.4K,+-5%,.125W,200PPM,1206	746495	89536	746495	1	
R 20	RES,CERM,1.6K,+-5%,.125W,200PPM,1206	746446	89536	746446	1	
R 21	RES,CERM,5.1K,+-5%,.125W,200PPM,1206	746560	91637	CRCW1206-5101JB02	1	
R 22, 23	RES,CERM,22,+-5%,.125W,200PPM,1206	746230	91637	CRCW1206-22ROJB02	2	
R 24, 25	RES,CERM,10K,+-5%,.125W,200PPM,1206	746610	91637	CRCW1206-1002JB02	2	
TP 1- 10	TERM,UNINSUL,WIRE FORM,TEST POINT	781237	27918	TP102-01	10	
U 1	✓ IC,NMOS,ADV VIDEO DISPLAY CNTRLR,PLCC	742734	18324	SCN2674BC4A44T	1	
U 2	✓ IC,BIPOLAR,CLR/MONO ATTRI CNTRLR,PLCC	742742	18324	SCB2675BC5A44T	1	
U 3, 4	✓ IC,2K X 8 STATIC RAM,120NSEC,SOIC	742783	65786	CY7C128-55SC	2	
U 5	✓ PROGRAMMED 27128-150 V2.0	818195	89536	818195		
U 6- 8	✓ IC,FTTL,QUAD 2-1 LINE MUX,SOIC	773028	18324	74F157ADT	3	
U 9, 10	✓ IC,LSTTL,OCTL LINE DRVR,SOIC	742122	18324	N74LS244DT	2	
U 11, 12	✓ IC,LSTTL,OCTL D TRNSPRNT LATCHES,SOIC	742726	01295	SN74LS373DR	2	
U 13	✓ IC,LSTTL,OCTAL D F/F,+EDG TRG,SOIC	741975	18324	N74LS374DT	1	
U 14	✓ IC,LSTTL,QUAD D F/F,+EDG TRG,SOIC	742619	01295	SN74LS175ADR	1	
U 15	✓ IC,STTL,QUAD D F/F,+EDG TRG,SOIC	742700	01295	SN74S175DR	1	
U 16- 19	✓ IC,LSTTL,QUAD 2 INPUT NAND GATE,SOIC	741033	18324	N74LS00DT	4	
U 20, 21	✓ IC,LSTTL,TRIPLE 3 INPUT AND GATE,SOIC	741264	18324	N74LS10D	2	
U 22	✓ IC,LSTTL,HEX INVERTER,SOIC	741017	18324	N74LS04DT	1	
U 23	✓ IC,LSTTL,SINGLE 8-INP. NAND GATE,SOIC	742510	01295	SN74LS30DR	1	
U 24	✓ IC,ALSTTL,DUAL JK F/F,-EDG TRG,SOIC	807578	01295	SN74ALS112ADR	1	
U 25	✓ IC,STTL,QUAD 2 INPUT +OR GATE,SOIC	742692	01295	74S86DR	1	
U 26	✓ IC,LSTTL,QUAD 2 INPUT AND GATE,SOIC	740860	18324	M74LS08DT	1	
U 27	✓ IC,LSTTL,OCTAL BUFFER INVERTED,SOIC	742627	01295	SN74LS240DR	1	
U 28	✓ ISOLATOR,OPTO,DUAL,DTL/TTL COMPATABLE	418285	28480	HCPL-2630	1	
U 29- 31	✓ ISOLATOR, 20 MHZ OPTOCOUPLER	742817	28480	HCPL-2400,OPTION 100	3	
XU 5	SOCKET,IC,28 PIN	448217	91506	228-AG39D	1	
XY 1	INSUL PART,DIP SOCKET,NYL,14 PIN	441865	32559	814-060	1	
XZ 1, 2	SOCKET,IC,16 PIN	276535	00779	2-640358-1	2	
Y 1	OSCILLATOR,31.9399 MHZ,TTL CLOCK	800029	89536	800029	1	
Z 1	JUMPER,DIP,0.300CTR,PROGRAM, 8 POS	783183	51167	16-680-191T	1	
NOTES:	✓ Static sensitive part.					

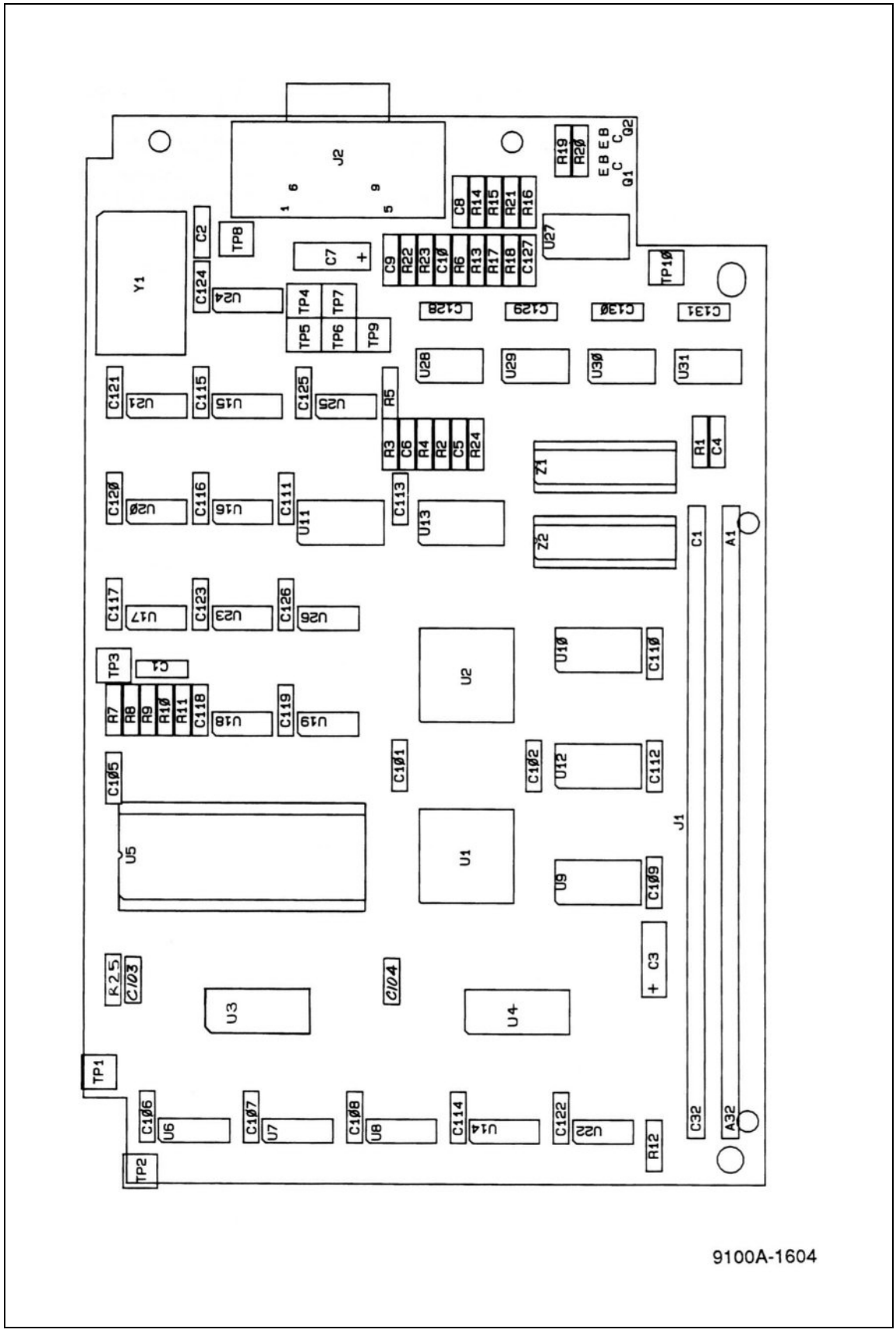


Figure 5-5. A4 Video Controller PCA

Table 5-5. A5 Probe Assembly

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 1	CAP,CER,27PF,+-10%,50V,COG,1206	800508	04222	12065A270KAT060B	1	
C 2, 5	CAP,CER,1000PF,+-10%,50V,COG,1206	747378	04222	12065A102KAT060B	2	
C 3, 4, 6	CAP,CER,0.22UF,+80-20%p50V,Y5V,1206	740597	51406	GRM42-Y5U221Z050PB	3	
CR 1	✓ DIODE,SI,BV=40V,IO=0.2A,MLF	851878	15238	LL103A	1	
CR 2- 5	✓ DIODE,SI,BV=75.0V,IO=100MA,MLF	742064	8A233	BAS32	4	
CR 6	LED,RED,T1-3/4,12 MCD	876453	28480	HLMP-3366	1	
CR 7	LED,YELLOW,T1-3/4,12 MCD	876458	28480	HLMP-3466	1	
CR 8	LED,GREEN,T1-3/4,10.6 MCD	876461	28480	HLMP-3568	1	
MP 1	CONNECTOR, GROUND CLIP, FINISHED	788026	89536	788026	1	
MP 2	COVER, PROBE	773309	89536	773309	1	
MP 3	KEYTOP	773333	89536	773333	1	
MP 4	BODY, PROBE	773317	89536	773317	1	
MP 5	LABEL,ADHES,MYLAR,BAR CODE,1.25,.245	807099	9R216	807099	1	
Q 1, 2	✓ TRANSISTOR,SI,PNP,SMALL SIGNAL,SOT-23	742023	73445	BCX17TRL	2	
Q 3, 4	✓ TRANSISTOR,SI,NPN,SMALL SIGNAL,SOT-23	742031	73445	BCX19TRL	2	
R 1	✓ RES,CERM,220,+-5%,.125W,200PPM,1206	746347	91637	CRCW1206-2200JB02	1	
R 2	✓ RES,CERM,100K,+-1%,.125W,l00PPM,1206	769802	91637	CRCW1206-104FB02	1	
R 3, 8, 10	✓ RES,CERM,200,+-5%,.125W,200PPM,1206	746339	91637	CRCW1206-2000JB02	3	
R 4	✓ RES,CERM,330,+-5%,.125W,200PPM,1206	746370	91637	CRCW1206-3300JB02	1	
R 5- 7	✓ RES,CERM,470,+-5%,.125W,200PPM,1206	740506	91637	CRCW1206-4700JB02	3	
R 9	✓ RES,CERM,205K,+-1%,.125W,lOOPPM,1206	769836	91637	CRCW1206-2053FB02	1	
R 14- 16	✓ RES,CERM,270,+-5%,.125W,200PPM,1206	746354	91637	CRCW1206-2700JB02	3	
S 1	SWITCH,PUSHBUTTON,SPST,MOMENTARY	782656	72884	SKHHAM	1	
U 1	✓ IC,FTTL,HEX INVERT W/SCHMT TRIG,SOIC	742825	18324	N74F14D	1	
W 1	CABLE ASSY, PROBE	853064	89536	853064	1	
NOTES:	✓ static sensitive part.					

Table 5-5a. A5 Probe Accessories Kit

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
MP 1	CLIP,HOOK,6-32 INSERT,BLACK	602938	89536	602938	1	
MP 2	CLIP,HOOK,W/0.025 PIN INTERFACE,BLACK	757500	05276	4521-0	8	
MP 3	TIP PROBE, FINISHED	788018	89536	788018	5	
W 1	GROUND WIRE ASSY	609115	89536	609115	1	
W 2	CABLE ASSEMBLY, TIP CONTACT	773408	89536	773408	1	

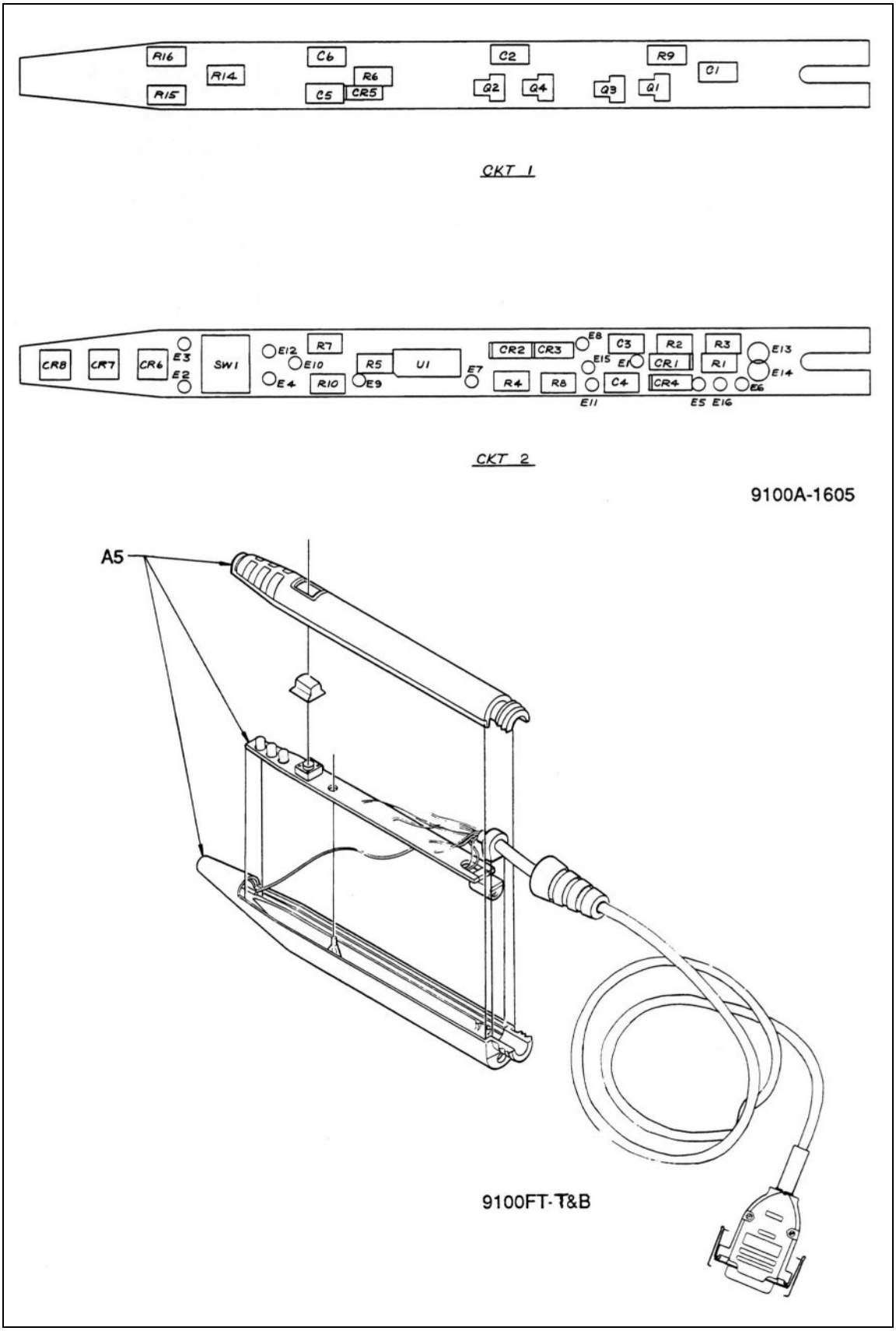


Figure 5-6. A5 Probe Assembly

Table 5-6. A6 Clock Module PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 1- 4	CAP,CER,8.2PF,+-10%,50V,COG,l206	747303	04222	12065A8R2KAT050B	4	
C 5- 12, 14	CAP,CER,0.01UF,+-l0%,50V,X7R,1206	747261	04222	12065C103KAT060R	9	
C 13	CAP,TA,10UF,+-20%,25V	772491	56289	195D106X0025G2B	1	
C 15	CAP,CER,1800PF,+-10%,50V,COG,1206	769786	04222	12065Al82KAT060B	1	
CR 1- 4	↯ DIODE,SI,BV=70.0V,IO=50MA,DUAL,SOT23	742320	8A233	BAV99	4	
J 1- 5	PIN,SINGLE,PWB,0.058 DIA	233411	00779	60599-3	5	
J 6	HEADER,2 ROW,.100CTR,RT ANG,16 PIN	417030	00779	87230-8	1	
MP 1	HLDR PART,FUSE,BODY,PWB MT	602763	61935	FAU031.3573	1	
MP 2	LABEL,ADHES,MYLAR,BAR CODE,1.25,.245	807099	9R216	807099	1	
R 1- 8	RES,CERM,22K,+-5%,.125W,200PPM,1206	746651	91637	CRCW1206-2202JB02	8	
R 9- 12	RES,CERM,11K,+-5%,.125W,250PPM,1206	769752	91637	CRCW1206-1102JB02	4	
R 13, 24- 27	RES,CERM,100,+-5%,.125W,200PPM,1206	746297	91637	CRCW1206-1000JB02	5	
R 14	RES,CERM,16K,+-5%,.125W,200PPM,1206	769745	91637	CRCW1206-163J B	1	
R 15- 22	RES,CERM,330,+-5%,.125W,200PPM,1206	746370	91637	CRCW1206-3300JB02	8	
R 23	RES,CERM,10K,+-5%,.125W,200PPM,1206	746610	91637	CRCW1206-1002JB02	1	
U 1, 2	↯ IC,COMPRTR,DUAL,HI-SPEED,16 PIN DIP	782219	6U095	AM687ADL	2	
XU 1, 2	SOCKET,IC,16 PIN	276535	00779	2-640358-1	2	
NOTES:	↯ Static sensitive part.					

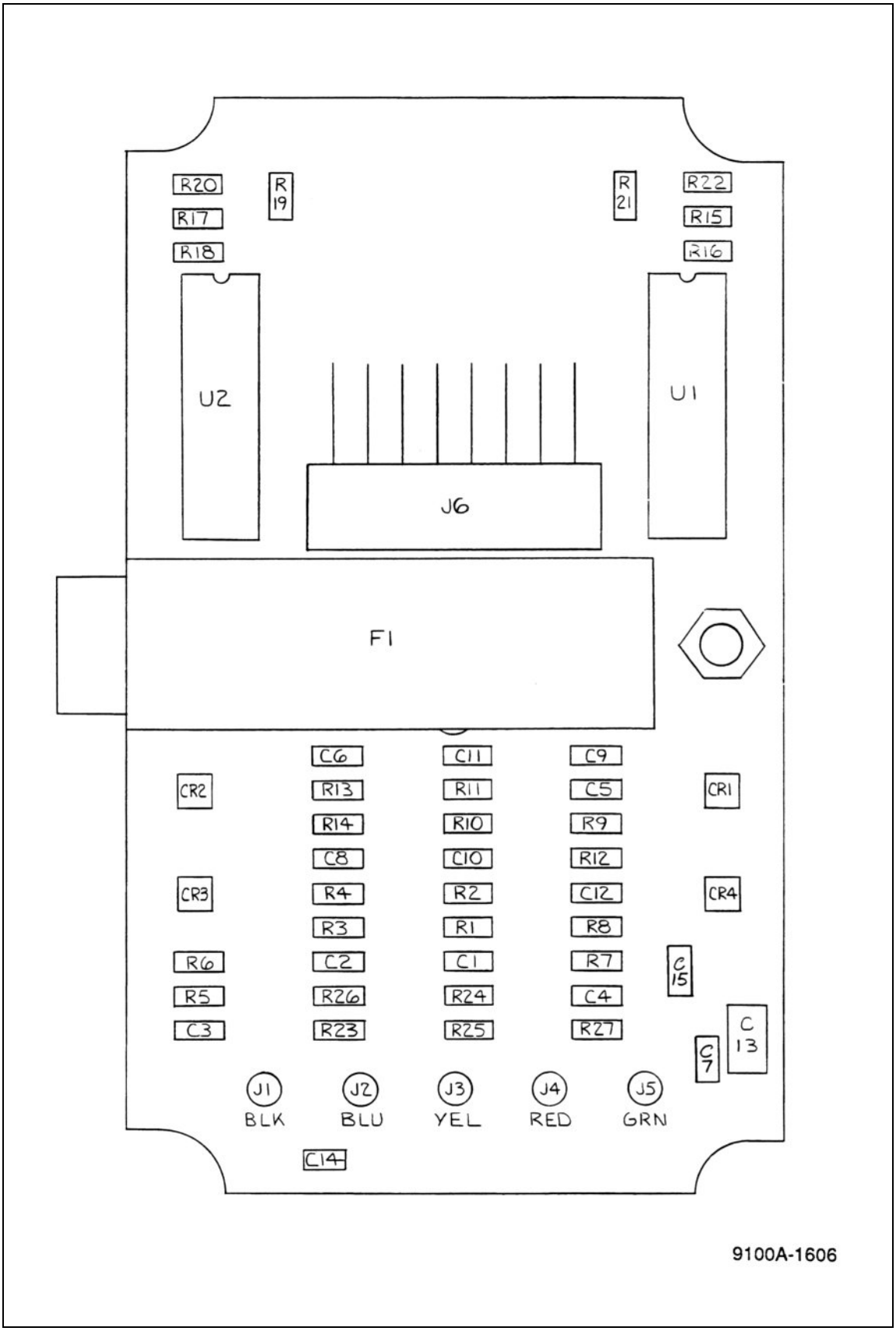


Figure 5-7. A6 Clock Module PCA

Table 5-7. A7 I/O Module (Main) PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 1, 2, 9-	CAP,TA,lOUF,+-20%,25V	772491	56289	195D106X0025G2B	27	
C 24, 27, 37,		772491				
C 42- 44, 61,		772491				
C 62, 67, 68		772491				
C 3- 7, 28-	CAP,CER,0.01UF,+-10%,50V,X7R,1206	747261	04222	12065C103KAT060R	23	
C 36, 38, 39,		747261				
C 46, 55- 60		747261				
C 45	CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287	04222	12063C104KAT060B	1	
CR 1- 4, 7,	✗ DIODE,SI,BV=70.0V,IO=50MA,DUAL,SOT23	742320	8A233	BAV99	85	
CR 100-163	✗	742320				
CR 5, 6	✗ DIODE,SI,BV=75.0V,IO=100MA,MLF	742064	8A233	BAS32	2	
CR 8	✗ DIODE,SI,SCHOTTKY,30V,1.1A,SOT89	782573	59993	10JQ030TRRM	1	
E 1- 8	TERM,UNINSUL,WIRE FORM,TEST POINT	781237	27918	TP102-01	8	
H 1	WASHER,FLAT,MYLAR,.200,.395,.010	161646		COMMERCIAL	1	
H 2	SCREW,PH,P,SEMS,STL,6-32,.250	178533		COMMERCIAL	1	
J 1	HEADER,2 ROW,.100CTR,RT ANG,38 PIN	782748	00779	1-87230-9	1	
J 2, 3	SOCKET,2 ROW,PWB,O.100CTR,30 POS	783795	00779	1-534236-5	2	
MP 1	HLDR PART,FUSE,BODY,PWB MT	602763	61935	FAU031.3573	1	
MP 2	SPACER,.312 HEX,AL,6-32,.625	104448	89536	104448	1	
MP 3	LABEL,ADHES,MYLAR,BAR CODE,1.25,.245	807099	9R216	807099	1	
P 1	HEADER,1 ROW,.150CTR,RT ANG,6 PIN	783803	89536	783803	1	
Q 1, 2	TRANSISTOR,SI,PNP,SMALL SIGNAL,SOT-23	742684	04713	NMBT3906T	2	
R 1, 2	RES,CERM,100,+-5%,.125W,200PPM,1206	746297	91637	CRCW1206-1000JB02	2	
R 3, 5, 6,	RES,CERM,l0K,+-1%,.125W,100PPM,1206	769794	91637	CRCW1206-103FB02	4	
R 10		769794				
R 4, 9	RES,CERM,42.2K,+-1%,.125W,lOOPPM,1206	769851	91637	CRCW1206-4222FB02	2	
R 7	RES,CERM,7.5K,+-1%,.125W,100PPM,1206	811463	91637	CRCW1206-752FB02	1	
R 8	RES,CERM,825,+-1%,.125W,100PPM,1206	811455	91637	CRCW1206-8250FB02	1	
R 13, 14	RES,CERM,9.1K,+-5%,.125W,200PPM,1206	746602	91637	CRCW1206-9101JB02	2	
R 15, 17, 41-	RES,CERM,43K,+-5%,.125W,200PPM,1206	769299	91637	CRCW1206-4302JB02	6	
R 44		769299				
R 16, 18	RES,CERM,910,+-5%,.125W,200PPM,1206	769257	91637	CRCW1206-9100JB02	2	
R 19, 20, 23-	RES,CERM,4.7K,+-5%,.125W,200PPM,1206	740522	91637	CRCW1206-4701JB02	10	
R 30		740522				
R 21, 22, 31,	RES,CERM,1K,+-5%,.125W,200PPM,1206	745992	91637	CRCW1206-1001JB02	7	
R 33, 34, 39,		745992				
R 40		745992				
R 32	RES,CERM,llK,+-5%,.125W,250PPM,1206	769752	91637	CRCW1206-1102JB02	1	
TP 1- 5	PIN,SINGLE,PWB,0.058 DIA	233411	00779	60599-3	5	
U 1	OSCILLATOR,1MHZ,TTL CLOCK	634113	91637	XO-43D 1	1	
U 2	✗ IC,OP AMP,QUAD,LOW POWER,SOIC	742569	18324	LM324D	1	
U 3, 5	✗ IC,LSTTL,QUAD 2 INPUT AND GATE,SOIC	740860	18324	N74LS08DT	2	
U 4	✗ IC,CMOS,HEX INVERTER,SOIC	742585	18324	N74HCT040	1	
U 6	✗ IC,LSTTL,3-8 LINE DCDR W/ENABLE,SOIC	740969	18324	M74LS138DT	1	
U 7	✗ IC,LSTTL,OCTL D TRNSPRNT LATCHES,SOIC	742726	01295	SN74LS373DR	1	
U 8	✗ IC,CMOS,OCTAL BUS TRANSCEIVER,SOIC	742577	01295	SN74HCT245DWR	1	
U 9	✗ IC,ECL,QUAD ECL-TTL TRANSLATOR,PLCC	852140	04713	MC10H125FN	1	
U 10	✗ IC,LSTTL,QUAD 2 INPUT OR GATE,SOIC	740878	18324	N74LS32D	1	
U 11, 12	✗ IC,LSTTL,DUAL JK F/F,-EDG TRIG,SOIC	741256	18324	N74LS112DT	2	
U 13, 16, 17	✗ IC,CMOS,OCTL LINE DRVR,SOIC	742593	01295	SN74HCT244DWR	3	
U 14	✗ IC,LSTTL,OCTAL D F/F,+EDG TRG,SOIC	740928	18324	N74LS273DT	1	
U 15	✗ IC,LSTTL,SINGLE 8-INP. NAND GATE,SOIC	742510	01295	SN74LS30DR	1	
U 18	✗ IC,CMOS,DUAL 4-1 SELECT/MUX,SOIC	780767	18324	74HCT153DT	1	
U 100,110,120,	✗ IC MOS QUEST 9000 CHIP PLASTIC TEST	754499	89536	754499	5	
U 130,140	✗	754499				

Table 5-7. A7 I/O Module (Main) PCA (cont)

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
U 101,103,111,	↯ TRANSISTOR,SI,P-DMOS,QUAD,POWER,SOIC	854146	89536	854146	10	
U 113,121,123,	↯	854146				
U 131,133,141,	↯	854146				
U 143	↯	854146				
U 102,104,112,	↯ TRANSISTOR,SI,N-DMOS,QUAD,POWER,SOIC	854153	89536	854153	10	
U 114,122,124,	↯	854153				
U 132,134,142,	↯	854153				
U 144	↯	854153				
U 105,106,115,	↯ IC,CMOS,OCTL LINE DRVR,SOIC	801043	04713	MC74HC244ADWR1	10	
U 116,125,126,	↯	801043				
U 135,136,145,	↯	801043				
U 146	↯	801043				
XY 1	INSUL PART,DIP SOCKET,NYL,14 PIN	441865	32559	814-060	1	
Z l,100,110,	RES,CERM,SOIC,16 PIN,8 RES,100,+-2%	838086	91637	SOMC-1603-101G	6	
Z 120,130,140		838086				
NOTES:	↯ Static sensitive part.					

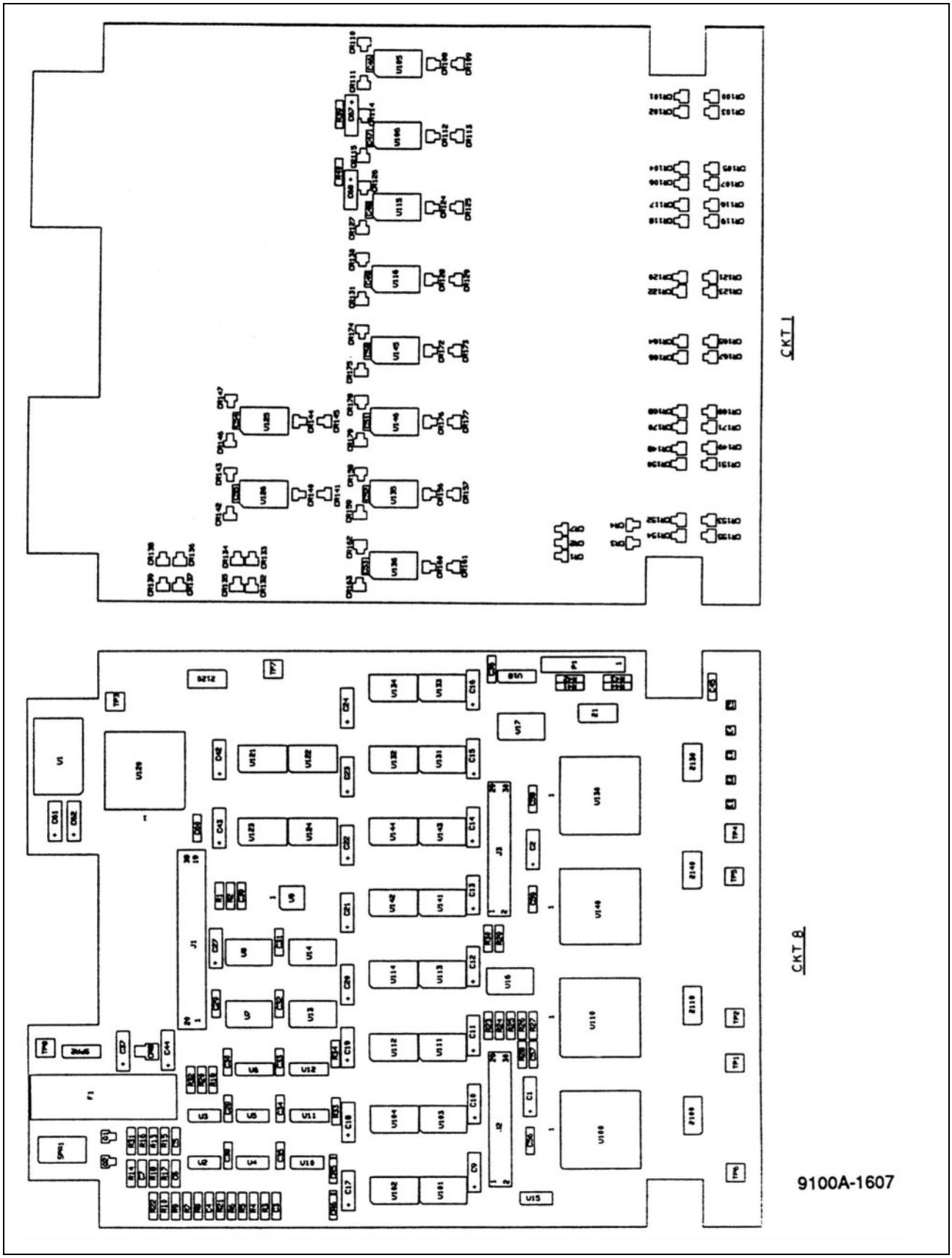


Figure 5-8. A7 I/O Module (Main) PCA

Table 5-8. A8 I/O Module (Top) PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 1- 4	CAP,AL,4700UF,+-20%,16V,SOLV PROOF	800904	89536	800904	4	
CR 1- 4	DIODE,SI,100 PIV,1.0 AMP	343491	04713	1N4002	4	
H 1	SCREW,PH,P,SEMS,STL,6-32,.250	178533		COMMERCIAL	2	
H 2	SCREW,PH,P,STL,SEMS,4-40,.187	732750		COMMERCIAL	4	
J 1, 4	HEADER,2 ROW,.100CTR,30 PIN	801233	89536	801233	2	
J 2, 3	CONN,RECT,PWB,REC,33 POS	800672	50541	KA33/127BPFD21TAHF6	2	
MP 1	COVER, SHIELD I/O MODULE	768036	89536	768036	1	
MP 2	LABEL,ADHES,MYLAR,BAR CODE,1.25,.245	807099	9R216	807099	1	
MP 3	SPACER,SWAGED,.250 RND,BR,6-32,.590	811224	9W423	9538B-B-0632	5	
MP 4	SACER,SWAGE,.250 RND,BR,6-32,.250	446351	9W423	9533B-B-0440	2	
P 1- 4	GUIDE SOCKET	805648	89536	805648	4	
NOTES:	↯ Static sensitive part.					

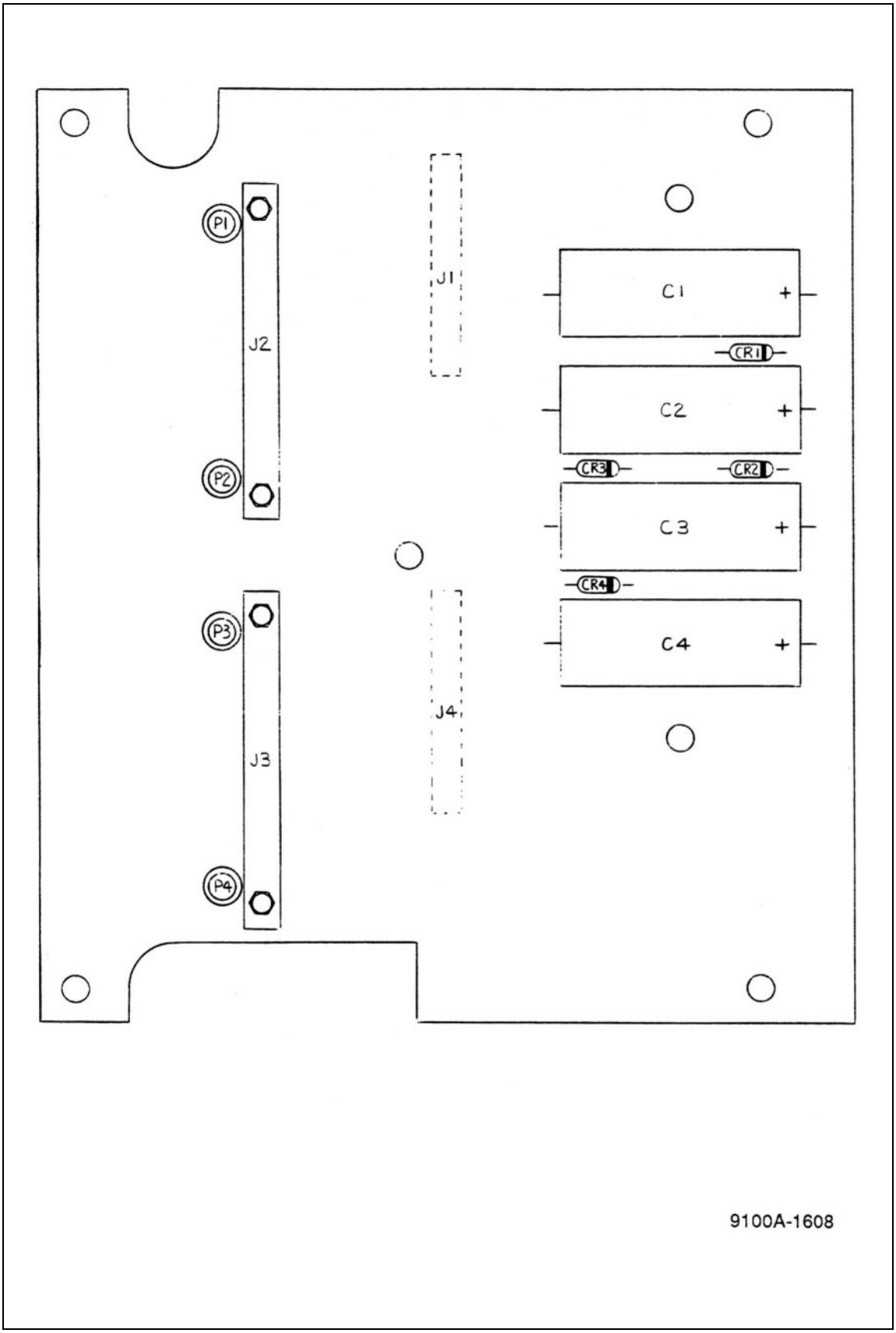


Figure 5-9. A8 I/O Module (Top) PCA

Table 5-9. A11 I/O Connector PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 1, 17	CAP,AL,l000UF,+50-20%,35V	641217	62643	SM35VB-1000	2	
C 2- 15	CAP,CER,0.01UF,+-20%,lOOV,X7R	407361	04222	SR201C103MAT	14	
C 16	CAP,AL,l0000UF,+-20%,6.3V,SOLV PROOF	800045	62643	SME6.3T103N16X40LL	1	
CR 1, 2	DIODE,SI,100 PIV,1.0 AMP	343491	04713	1N4002	2	
H 1	SCREW,PH,P,STL,LOCK,6-32,.250	152140	73734	19042	2	
H 2	SCREW,THD CUT,PH,P,SS,4-24,.375	183574		COMMERCIAL	2	
J 1	CONN,DIN41612,TYPE R,RT ANG,64 SCKT	782102	00779	531796-2	1	
J 2- 5	CONN,D-SUB,PWB,37 SCKT	782177	00779	2-747709-0	4	
MP 1	HEAT DIS,HORIZ,1.63X1.29X1.00,TO-66	799965	30161	ER5758B	1	
MP 2	LABEL,ADHES,MYLAR,BAR CODE,1.25,.245	807099	9R216	807099	1	
MP 3	LABEL,ADHES,MYLAR,.900,.200	854088	22670	GM027815	1	
R 1	RES,CP,lOK,+-5%,0.25W	348839	59124	CF1-4 102 J B	1	
R 3	RES,WW,0.47,+-5%,2W	219360	23237	SPH470J	1	
R 4	RES,MF,243,+-0.1%,0.125W,50PPM	512228	91637	CMF-55 2430B T-2	1	
R 5	RES,MF,732,+-1%,0.125W,100PPM	294884	91637	CMF-55 7320F T-1	1	
TP 1	TERM,UNINSUL,WIRE FORM,TEST POINT	781237	27918	TP102-01	1	
U 1, 2	✗ IC,ECL,QUAD TTL-ECL TRANSLATOR	801266	04713	MC10H124P	2	
U 3	✗ IC,LSTTL,DUAL 4 INPUT NAND GATE	393280	01295	SN74LS20N	1	
U 4	✗ IC,VOLT REG,ADJ,1.2 TO 32 V,5 AMP OUT	585497	27014	LM338K	1	
Z 1, 3	RES,CERM,SIP,10 PIN,9 RES,330,+-2%	769364	91637	CSC10A-01-331G	2	
Z 2	RES,CERM,SZP,10 PIN,9 RES,4.7K,+-2%	484063	91637	CSC10A-01-472G	1	
NOTES:	✗ Static sensitive part.					

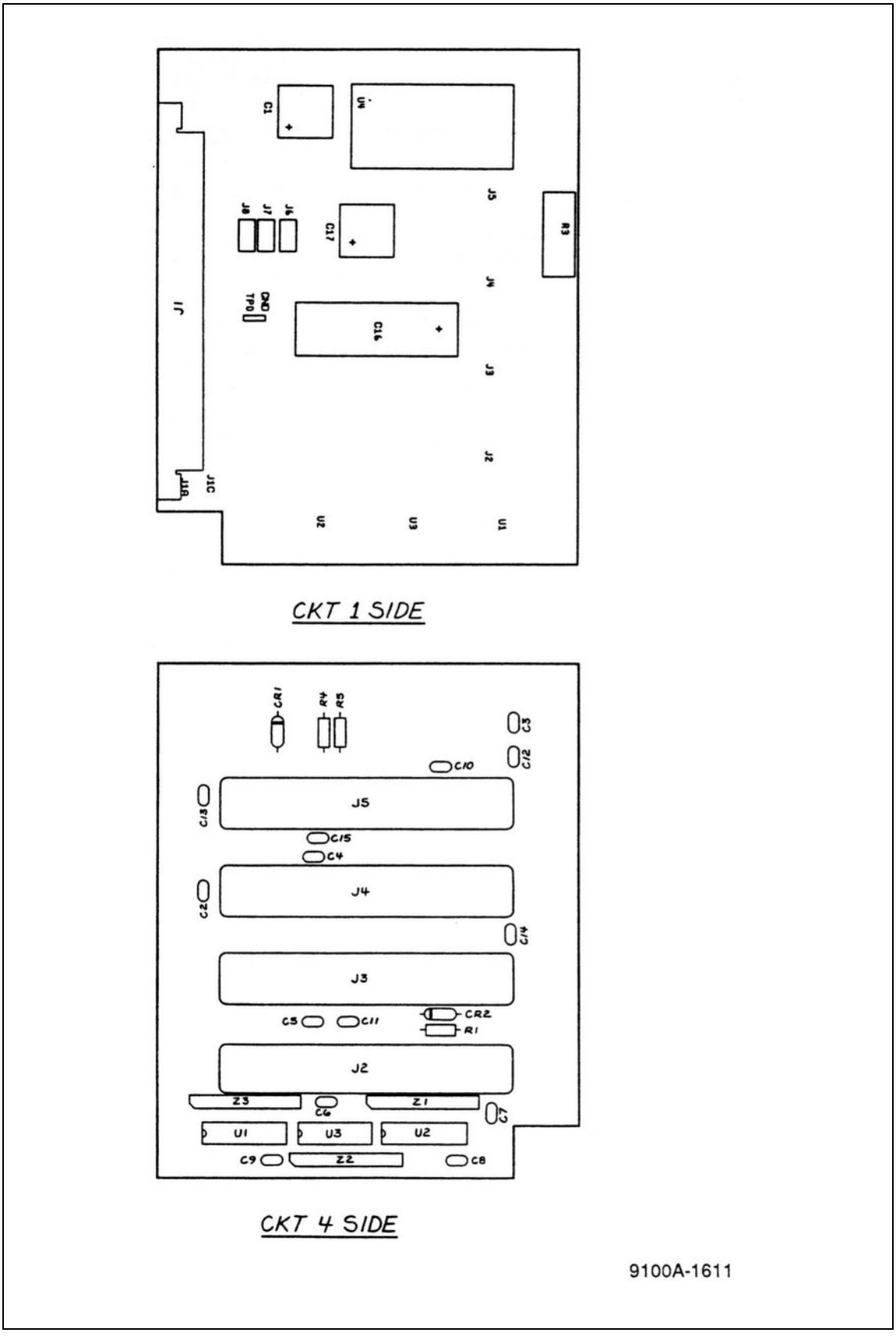


Figure 5-10. A11 I/O Connector PCA

Table 5-10. A12 Half-Width Clip Modules

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 1	CAP,CER,0.1UF,+-20%,50V,Z5U	597575	89536	597575	1	
C 2	CAP,CER,0.01UF,+-20%,100V,X7R	407361	72982	8121-A100-WSR-103M	1	
H 1	SCREW, MACH, PHP, STL, 4-40 X 5/8	800656	89536	800656	4	
J 1	CONN,RECT,PWB,PLUG,33 POS	800680	89536	800680	1	
J 2, 3	CONNECTOR ASSY		89536		2	1
MP 1	CLIP,TEST,IC		89536		1	1
MP 2	CLIP,HOOK,W/0.025 PIN INTERFACE,BLACK	757500	89536	757500	1	
MP 3	BUTTON, SWITCH	773895	89536	773895	1	
MP 4	MODULE BOTTOM, SINGLE	766697	89536	768697	1	
MP 5	MODULE TOP, SINGLE	774034	89536	774034	1	
MP 6	KEY		89536		2	1
MP 7	MODULE DECAL		89536		1	1
P 1, 2	BANANA PLUG,PWB,SOLDER OR SWAGE TYPE	800698	89536	800698	2	
S 1	SWITCH,PUSHBUTTON,SPST,MOMENTARY	782433	89536	782433	1	
S 2	SWITCH,DIP,SPST,4 POS	408559	00779	435166-2	1	
W 1	CABLE SET ASSY		89536		1	1
W 2	WIRE ASSY, GROUND CLIP	801704	89536	801704	1	

NOTES:

1 - Refer to the table below for appropriate part numbers for each type of Clip Module:

	MODULE								
	-14D	-14S	-16D	-16S	-18D	-20D	-20S	-24D	-24S
MP1	800052	817429	800060	817437	800078	800086	817445	800094	817478
W1	801639	801639	801647	801647	801654	801662	801662	801670	801670
J2,3	801878	801878	801886	801886	801894	801902	801902	801910	801910
MP6	-	-	-	-	773952	773952	773952	767954	767954
MP7	802140	819631	802157	819649	802165	802173	819656	802181	819664

Table 5-11. A13 Full-Width Clip Modules

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 1, 4	CAP,CER,0.01UF,+-20%,l00V,X7R	407361	72982	8121-A100-W5A-103M	2	
C 2, 3	CAP,CER,0.1UF,+-20%,50V,Z5U	597575	89536	597575	2	
H 1	SCREW, MACH, PHP, STL, 4-40 X 5/8	800656	89536	800656	4	
J 1, 2	CONN,RECT,PWB,PLUG,33 POS	800680	89536	800680	2	
J 3, 4	CONNECTOR ASSY, 20 PIN		89536		2	1
MP 1	CLIP,TEST,IC		89536		1	1
MP 2	CLIP,HOOK,W/0.025 PIN INTERFACE,BLACK	757500	89536	757500	1	
MP 3	BUTTON, SWITCH	773895	89536	773895	1	
MP 4	MODULE BOTTOM, DOUBLE	802132	89536	802132	1	
MP 5	MODULE TOP, DOUBLE	802124	89536	802124	1	
MP 6	KEY, EXTENDED	767954	89536	767954	2	
MP 7	MODULE DECAL		89536		1	1
P l, 4	BANANA PLUG,PWB,SOLDER OR SWAGE TYPE	800698	89536	800698	2	
S 1	SWITCH,PUSHBVTTON,SPST,MOMENTARY	782433	89536	782433	1	
S 2	SWITCH,DIP,SPST,8 POS	414490	00779	435166-5	1	
W 1	CABLE SET ASSY		89536		1	1
W 2	WIRE ASSY, GROUND CLIP	801704	89536	801704	1	

NOTES:

1 - Refer to the table below for appropriate part numbers for each type of Clip Module:

	MODULE -28D	-28S	-40D
MP1	800102	821975	800110
W1	801688	801688	801696
J3, 4	801928	801928	801936
MP7	802199	819672	802207

Table 5-12. A14 Calibration Module

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
H 1	SCREW,PH,P,SS,4-40,.625	800656		COMMERCIAL	7	
J 1, 2	CONN,RECT,PWB,PLUG,33 POS	800680	50541	KA33/127BPMD11T	2	
MP 1	TEST LEAD,PVC,HOOK-HOOK,BLK	801050	05276	E11395-36-0	1	
MP 2	CABLE ACCESS,TIE,4.00L,.10W,.75 DIA	172080	06383	SST-1M	2	
MP 3	BUTTON, SWITCH	773895	89536	773895	1	
MP 4	MODULE BOTTOM, DOUBLE	802132	89536	802132	1	
MP 5	MODULE TOP, DOUBLE	802124	89536	802124	1	
MP 6	KEY, EXTENDED	767954	89536	767954	2	
MP 7	MODULE DECAL, CALIBRATION	802223	22670	802223	1	
MP 8	LABEL,ADHES,MYLAR,BAR CODE,1.25,.245	807099	9R216	807099	1	
P 1, 2	BANANA PLUG,PWB,SOLDER OR SWAGE TYPE	800698	18310	01-2258-2	2	
S 1	SWITCH,PUSHBUTTON,SPST,MOMENTARY	782433	61964	B3F-3122	1	
NOTES:	↯ Static sensitive part.					

Table 5-13. A15 Flying Lead Module

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 1	CAP,CER,0.1UF,+-20%,50V,Z5U	597575	89536	597575	1	
C 2	CAP,CER,0.01UF,+-20%,l00V,X7R	407361	04222	SR201C103MAT	1	
H 1	SCREW,PH,P,SS,4-40,.625	800656		COMMERCIAL	4	
J 1	CONN,RECT,PWB,PLUG,33 POS	800680	50541	KA33/127BPMD11T	1	
MP 1	CLIP,HOOK,W/0.025 PIN INTERFACE,BLACK	757500	05276	4521-0	25	
MP 2	BUTTON, SWITCH	773895	89536	773895	1	
MP 3	MODULE BOTTOM, SINGLE	768697	89536	768697	1	
MP 4	MODULE TOP, SINGLE	774034	89536	774034	1	
MP 5	KEY, FLUSH	773952	89536	773952	2	
MP 6	MODULE DECAL, 20FLS	802215	22670	802215	1	
S 1	SWITCH,PUSHBUTTON,SPST,MOMENTARY	782433	61964	B3F-3122	1	
S 2	SWITCH,DIP,SPST,4 POS	408559	00779	435166-2	1	
W 1	CABLE ASSEMBLY, 10 PAIR, POS 11-20	801720	89536	801720	1	
W 2	CABLE ASSY, 10 PAIR, POS 1-10	801712	89536	801712	1	
NOTES:	↙ Static sensitive part.					

Table 5-14. A19 Monochrome Monitor

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
BT 1	PWR SUP,35W,+5V,+12V,-12V	794214	89536	794214	1	
BT 2	DISPLAY MONITOR,GREEN SVC REQ	785414	89536	785414	1	
H 1	SCREW,PH,P,STL,LOCK,10-32,.375	114314	89536	114314	4	
H 2	WASHER,FLAT,STL,.203,.434,.031	110262	86928	5702-16-31	3	
H 3	WASHER,FLAT,STL,.149,.375,.031	110270	86928	5202-12-31	8	
H 4	SCREW,PH,P,STL,LOCK,6-32,.375	152165	73734	19044	8	
H 5	SCREW,PH,P,SEMS,STL,6-32,.375	177022		COMMERCIAL	12	
H 7	SCREW,PH,P,SEMS,STL,4-40,.250	185918		COMMERCIAL	6	
H 8	CONN ACC,D-SUB,LATCH BLOCK,SHORT,4-40	783480	00779	745403-9	2	
H 9	SCREW,PH,P,STL,LOCK,6-32,1.000	114215	89536	114215	3	
H 10	WASHER,FLAT,BRASS,#6,0.028 THK	111310	73734	1444	3	
MP 1	BRACKET, CRT, FINISHED PH2	849187	89536	849187	4	
MP 2	LABEL,ADHES,MYLAR,BAR CODE,1.25,.245	807099	9R216	807099	2	
MP 3	CHASSIS,FINISHED	794156	89536	794156	1	
MP 4	SPACER,SNAP,PWB,NYL,.312	780619	02768	215-150913-01	3	
MP 5	BEZEL ASSY,9100	792903	89536	792903	1	
MP 6	GASKET,TOUCH PANEL,DUST	843250	2K262	843250	1	
MP 7	NAMEPLATE	787275	22670	787275	1	
MP 8	ASSY, AC POWER PANEL	776377	89536	776377	1	
MP 9	COVER,CHASSIS,9100,FINISHED	794198	89536	794198	1	
MP 10	DAMPER, VIBRATION	805085	2K262	805085	4	
MP 11	CABLE TIE ANCHOR,ADHSV,.160TIE	407908	06383	ABMM-A-C	5	
MP 12	CABLE ACCESS,TIE,4.00L,.10W,.75 DIA	172080	06383	SST-1M	8	
MP 13	DECAL,COVER,9100	792911	89536	792911	1	
MP 14	DECAL, FAN PANEL	785493	22670	785493	1	
MP 15	BRACKET,POT MOUNTING,FINISHED	794131	89536	794131	1	
MP 16	THUMBWHEEL, POTENTIOMETER	787358	89536	787358	1	
MP 17	NAMEPLATE, SERIAL -REAR PANEL-	472795	85480	472795	1	
MP 18	SHIPPING BOX	776435	89536	776435	1	
MP 19	SHIPPING INSERT	777045	89536	777045	1	
MP 20	OPTION BOX ASSEMBLY	801613	89536	801613	1	
MP 21	SHIPPING CARRIER/INSERT	777052	89536	777052	1	
MP 22	ENCLOSURE W/GRILLS	802454	28406	802454	1	
MP 23	COVER, FAN	787366	89536	787366	1	
MP 24	DECAL, CAUTION	787242	22670	787242	1	
MP 25	BASE	747972	28406	747972	1	
MP 26	RETAINER, NUT	749655	28406	749655	1	
MP 27	BUSHING COVER RF OUTPUT	802553	89536	802553	1	
MP 28	SHOULDER WASHER	792861	20584	792861	2	
MP 29	RETAINER PIN	802520	89536	802520	1	
MP 30	BASE, MOUNTING PLATE	747998	28406	747998	1	
MP 31	FOOT,RUBBER,ADHES,BLK,.50 DIA,.14 THK	513820	28213	SJ-5012	4	
MP 32	PIN,MECHANICAL,CLEVIS,5/16 X 1-3/4	800524	96652	11-099	1	
MP 33	SPRING,COIL,COMP,M WIRE,.880,l.100	800532	83553	C1100-125-0880M	1	
MP 34	BUMPER,STEM,BUNA-S,0.500X0.125	800839	2K262	6171	4	
MP 35	DECAL CSA	525527	22670	525527	1	
TM 1	1021-31 INSTRUCTION SHEET	804914	89536	804914	1	
W 1	CABLE ASSY,9100	778613	89536	778613	1	
W 2	CORD,LINE,5-15/IEC,3-18AWG,SVT,7.5 FT	284174	70903	17239	1	
NOTES:	✓ Static sensitive part.					

Table 5-15. A24 Multi-Function I/F II PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 1- 17	CAP,CER,0.01UF,+-10%,50V,X7R,1206	747261	04222	12065C103KAT060R	17	
C 18	CAP,TA,10UF,+-20%,25V	772491	56289	195D106X0025G2B	1	
H 1	SCREW,THD CUT,PH,P,SS,4-24,.375	183574		COMMERCIAL	2	
H 2	RIVET,POP,DOME,AL,0.125X0.316	423616	1B715	AD42AH	2	
J 1	CONN,DIN41612,TYPE R,RT ANG,96 SCKT	747816	00779	531796-1	1	
J 2	HEADER,2 ROW,.100CTR,RT ANG,50 PIN	783464	00779	1-103311-0	1	
J 3	HEADER,2 ROW,.100CTR,50 PIN	782201	00779	2-102973-5	1	
J 4	HEADER,2 ROW,.100CTR,24 PIN	831834	88245	70-24-03	1	
MP 1	LABEL,ADHES,MYLAR,.900,.200	854088	22670	GM027815	2	
MP 2	LABEL,ADHES,MYLAR,BAR CODE,1.25,.245	807099	9R216	807099	1	
MP 3	SCSI CONNECTOR BRACKET	768663	89536	768663	1	
R 2- 11	RES,CERM,4.7K,+-5%,.125W,200PPM,1206	740522	91637	CRCW1206-4701JB02	10	
TP 1- 3	TERM,UNINSUL,WIRE FORM,TEST POINT	781237	27918	TP102-01	3	
U 1	✓ IC,REAL TIME CLK W/ 50 X 8 STATIC RAM	866509	0B0A9	DS1287	1	
U 2	✓ IC,LSTTL,OCTAL GPIB XCVR,SOIC	831651	01295	SN75160BDWR	1	
U 3, 18	✓ IC,CMOS,HEX INVERTER,SOIC	838219	34371	CD74ACT04M	2	
U 4	✓ IC,LSTTL,8BIT S-IN,P-OUT R-SHFT,SOIC	742106	18324	NN74LS164DT	1	
U 5	✓ IC,NMOS,GPIB CONTROLLER,PLCC	887190	01295	TMS9914AFNLR	1	
U 6	✓ IC,CMOS,SMALL COMPTR SYS INTERFC,PLCC	866512	51809	53C80-44PL	1	
U 7	✓ IC,ALSTTL,OCTAL IEEE-488 BUS TRANSCVR	854950	01295	SN75ALS162DWR	1	
U 8, 11	✓ PROG'MD PAL SET, 20L8, V1.0, U8, U11	870352	89536	870352	2	
U 9, 13, 14,	✓ IC,CMOS,OCTAL BUS TRANSCEIVER,SOIC	742577	01295	SN74HCT245DWR	4	
U 17	✓	742577				
U 10	✓ IC,CMOS,OCTL LINE DRVR,SOIC	742593	01295	SN74HCT244DWR	1	
U 12	✓ IC,NMOS,DUAL DIR MEM ACC CNTRLR,PLCC	866454	04713	MC68440FN8	1	
U 15, 16	✓ IC,CMOS,OCTAL D TRANSPARNT LATCH,SOIC	830760	04713	MC74HCT373DWTR7	2	
Z 1, 2	RES,CERM,SIP,10 PIM,9 RES,220,+-2%	769356	91637	CSC10A-01-221G	2	
Z 3, 4	RES,CERM,SIP,10 PIN,9 RES,330,+-2%	769364	91637	CSC10A-01-331G	2	
NOTES:	✓ Static sensitive part.					

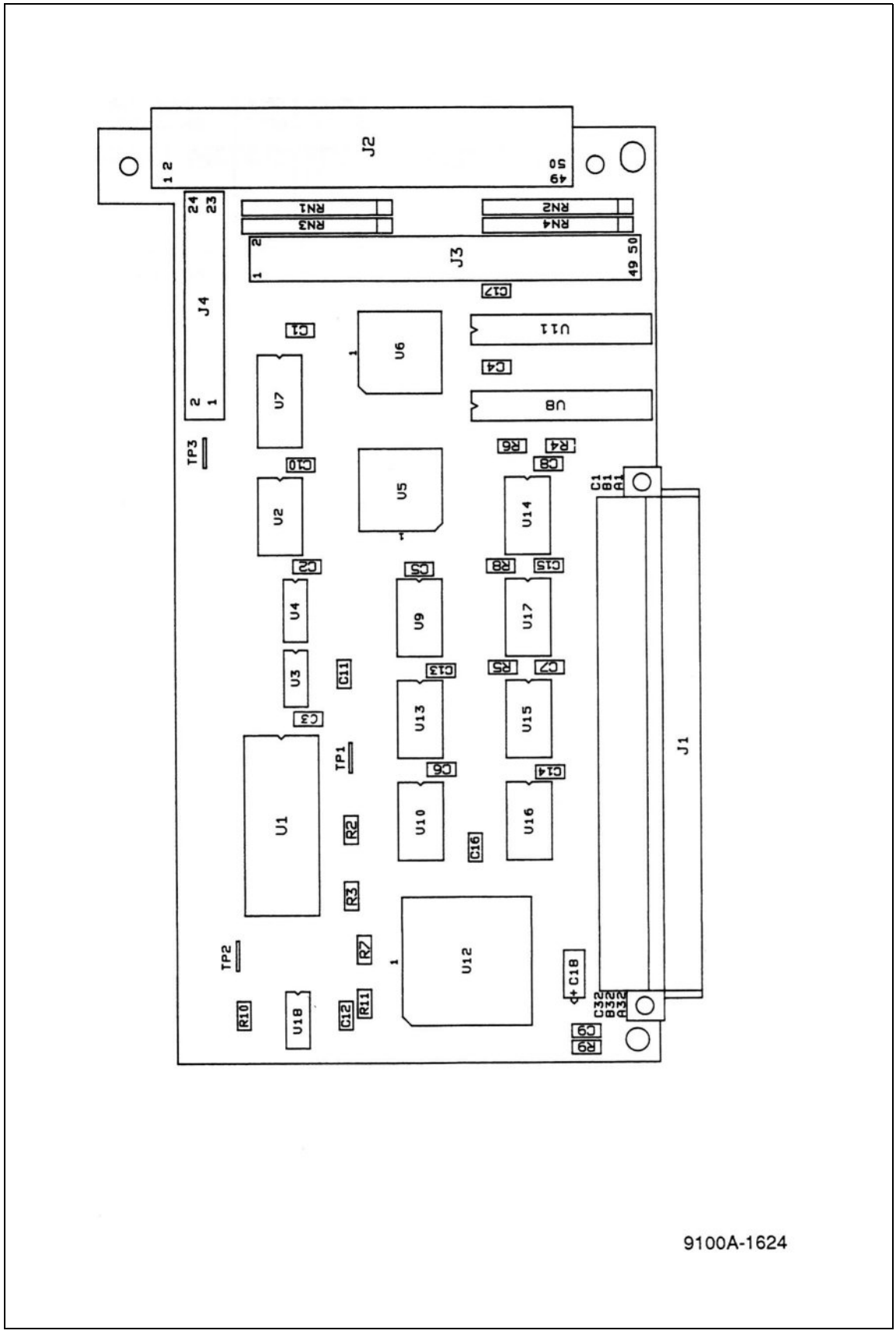


Figure 5-11. A24 Multi-Function I/F II PCA

Table 5-16. A25 Probe I/O-ECL PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 1, 3, 4, C 8- 11, 16, C 17, 19, 21, C 23, 25- 33 C 39, 40, 43, C 44	CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287 747287 747287 747287 747287 747287	04222	12063C104KAT060B	25	
C 2	CAP,VAR,6-50PF,50V,CER	714618	51406	TZ03Z500YR174	1	
C 5, 7, 20, C 22, 24, 35	CAP,TA,10UF,+-20%,25V	772491 772491	56289	195D106X0025G2B	6	
C 6, 14, 18	CAP,TA,1.5UF,+-20%,50V	780478	56289	195D155X0050F2B	3	
C 12	CAP,CER,180PF,+-10%,50V,COG,1206	769778	04222	12065A181KAT050R	1	
C 13	CAP,CER,33PF,+-10%,50V,COG,1206	769240	04222	12065A330KAT050B	1	
C 15	CAP,CER,0.022UF,+-10%,50V,X7R,1206	747279	04222	12065C223KAT060B	1	
C 34	CAP,CER,1500PF,+-10%,50V,COG,1206	781203	04222	12065A152KAT050R	1	
C 36	CAP,CER,470PF,+-10%,50V,COG,1206	747360	04222	12065A471KAT050B	1	
C 37, 38, 45	CAP,CER,0.01UF,+-10%,50V,X7R,1206	747261	04222	12065C103KAT060R	3	
C 41, 42	CAP,TA,47UF,+-20%,20V	348516	56289	199D476X0020EA2	2	
CR 1- 6, 8, CR 11	✓ DIODE,SI,BV=75.0V,IO=100MA,MLF ✓	742064 742064	8A233	BAS32	8	
CR 7, 9, 10	✓ DIODE,SI,BV=70.0V,IO=50MA,DUAL,SOT23	742320	8A233	BAV99	3	
CR 12	✓ DIODE,SI,SCHOTTKY,30V,1.1A,SOT89	782573	59993	10JQ030TRRM	1	
CR 13	✓ BANDGAP REF DIODE, 1.22V, 35PPM TC	634154	27014	LM385BX-1.2	1	
F 1	HLDR PART,FUSE,BODY,PWB MT	602763	61935	FAU031.3573	1	
J 1	CONN,D SUB,PWB,RT ANG,15 SCKT	782169	00779	747845-4	1	
J 2	CONN,DIN41612,TYPE R,64 PIN	782094	00779	532523-2	1	
J 3	CONN,D-SUB,PWB,RT ANG,15 PIN	782151	00779	747841-4	1	
J 4	HEADER,1 ROW,.100CTR,RT ANG,6 PIN	714154	00779	65521-106	1	
J 5	JACK,PWB,RT ANG,4 POS	782086	00779	520249-2	1	
J 6, 7	HEADER,2 ROW,.100CTR,40 PIN	603670	00779	2-102973-0	2	
J 8	HEADER,l ROW,.100CTR,4 PIN	867379	00779	102976-4	1	
MP 1	INSUL PART,TRANSISTOR MOUNT,DAP,TO-18	175125	07047	10172-DAP	1	
MP 2	LABEL,ADHES,MYLAR,BAR CODE,1.25,.245	807099	9R216	807099	1	
Q 1	✓ TRANSISTOR,SI,N-JFET,DUAL,TO-78	478370	21845	FD1838	1	
Q 2, 6, 9	✓ TRANSISTOR,SI,PNP,SMALL SIGNAL,SOT-23	742023	73445	BCX17TRL	3	
Q 3- 5	✓ TRANSISTOR,SI,NPN,SMALL SIGNAL,SOT-23	742031	73445	BCX19TRL	3	
Q 10, 11	✓ TRANSISTOR,SI,BV= 45V, 30W,TO-220	325761	34371	D44C5	2	
R 1	RES,CERM,33,+-5%,.125W,200PPM,1206	746248	91637	CRCW1206-33ROJB02	1	
R 2	RES,CERM,3.6K,+-5%,.125W,200PPM,1206	746537	91637	CRCW1206-362JB02	1	
R 3- 6, 48, R 49	RES,CERM,330,+-5%,.125W,200PPM,1206	746370 746370	91637	CRCW1206-3300JB02	6	
R 7	RES,CERM,150,+-5%,.125W,200PPM,1206	746313	91637	CRCW1206-1500JB02	1	
R 8	RES,CERM,15K,+-1%,.125W,100PPM,1206	769810	91637	CRCW1206-153FB02	1	
R 9, 90	RES,CERM,22,+-5%,.125W,200PPM,1206	746230	91637	CRCW1206-22R0JB02	2	
R 10- 12, 14, R 21, 28, 58	RES,CERM,470,+-5%,.125W,200PPM,1206	740506 740506	91637	CRCW1206-4700JB02	7	
R 13, 15	RES,CERM,200,+-5%,.125W,200PPM,1206	746339	91637	CRCW1206-2000JB02	2	
R 16, 46	RES,CERM,511,+-1%,.125W,l00PPM,1206	769869	91637	CRCW1206-5110FB02	2	
R 17, 20, 26, R 31, 36, 41, R 78	RES,CERM,1K,+-5%,.125W,200PPM,1206	745992 745992 745992	91637	CRCW1206-1001JB02	7	
R 18, 22, 23, R 27, 32- 34, R 37, 38, 42, R 52, 53, 55, R 62, 67, 72, R 80, 82, 86, R 91	RES,CERM,4.7K,+-5%,.125W,200PPM,1206	740522 740522 740522 740522 740522 740522 740522 740522	91637	CRCW1206-4701JB02	20	
R 19, 35, 84, R 85	RES,CERM,47K,+-5%,.125W,200PPM,1206	746685 746685	91637	CRCW1206-4702JB02	4	
R 24, 29, 30	RES,CERM,9.1K,+-5%,.125W,200PPM,1206	746602	91637	CRCW1206-9101JB02	3	
R 25	RES,CERN,3.9K,+-5%,.125W,200PPM,1206	746545	91637	CRCW1206-3900JB02	1	
R 39	RES,CERM,470K,+-5%,.125W,200PPM,1206	746792	91637	CRCW1206-4703JB02	1	
R 24, 29, 30	RES,CERM,9.1K,+-5%,.125W,200PPM,1206	746602	91637	CRCW1206-9101JB02	3	
R 25	RES,CERM,3.9K,+-5%,.125W,200PPM,1206	746545	91637	CRCW1206-3900JB02	1	
R 39	RES,CERM,470K,+-5%,.125W,200PPM,1206	746792	91637	CRCW1206-4703JB02	1	

Table 5-16. A25 Probe I/O-ECL PCA (cont)

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
R 40, 43, 45,	RES,CERM,100,+-5%,.125W,200PPM,1206	746297	91637	CRCW1206-1000JB02	6	
R 47, 79, 81		746297				
R 44	RES,CERM,270K,+-5%,.125W,200PPM,1206	876342	91637	CRCW1206-274JB02	1	
R 50, 57	RES,CERM,1.15K,+-1%,.125W,100PPM,1206	780981	91637	CRCW1206-2B1151FB02	2	
R 51, 59	RES,CERM,1.87K,+-1%,.125W,100PPM,1206	822312	91637	CRCW1206-1871FB02	2	
R 54, 56, 60	RES,CERM,1.21K,+-1%,.125%,100PPM,1206	867189	91637	CRCW1206-1211FB02	3	
R 64	RES,CERM,750,+-5%,.125W,200PPM,1206	746404	91637	CRCW1206-7500JB02	1	
R 65	RES,CERM,39K,+-5%,.125W,200PPM,1206	746677	91637	CRCW1206-3902JB02	1	
R 66	RES,CERM,3K,+-5%,.125W,200PPM,1206	746511	91637	CRCW1206-3001JB02	1	
R 68, 75	RES,CERM,30.1K,+-1%,.125W,100PPM,1206	801258	91637	CRCW1206-3012FB02	2	
R 69	RES,CERM,47,+-5%,.125W,200PPM,1206	746263	91637	CRCW1206-47R0JB02	1	
R 70	RES,CERM,3.4K,+-1%,.125W,100PPM,1206	769844	91637	CRCW1206-342FB02	1	
R 71, 74, 76	RES,CERM,10K,+-1%,.125W,100PPM,1206	769794	91637	CRCW1206-103FB02	4	
R 77		769794				
R 73	RES,CERM,620,+-5%,.125W,200PPM,1206	745984	91637	CRCW1206-6200JB02	1	
R 83	RES,CF,2.2,+-5%,0.25W	354944	59124	CF1-4 2R2 J B	1	
R 87	RES,CERM,1.30K,+-1%,.125W,100PPM,1206	780999	91637	CRCW1206-132FB02	1	
R 88	RES,CERM,243,+-1%,.125W,100PPM,1206	810606	91637	CRCW1206-2430FB02	1	
TP 1, 2, 5-7	TERM,UNINSUL,WIRE FORM,TEST POINT	781237	27918	TP102-01	5	
TP 7		781237				
U 1	✗ ISOLATOR, 20 MHZ OPTOCOUPLER	742817	28480	HCPL-2400,OPTION 100	1	
U 2	✗ IC,CMOS,QUAD 2 INPUT XOR GATE,SOIC	838391	34371	CD74ACT86M	1	
U 3	✗ IC,LSTTL,QUAD 2 INPUT NOR GATE,SOIC	741025	18324	N74LS02DT	1	
U 4, 12	✗ IC,FTTL,HEX INVERTER,SOIC	742148	18324	N74F04DT	2	
U 5	✗ IC,FTTL,QUAD DUAL AND GATE,SOIC	780957	18324	N7410DT	1	
U 6	✗ IC,CMOS,HEX INVERTER W/SCHT TRIG,SOIC	780965	18324	N74HCT14DT	1	
U 9	✗ IC,FTTL,QUAD 2-1 LINE MUX,SOIC	773028	18324	74F157ADT	1	
U 10	✗ IC,FTTL,DUAL D F/F,+EDG TRG,SOIC	742163	18324	74F74DT	1	
U 11	✗ IC,FTTL,QUAD 2 INPUT OR GATE,SOIC	743237	18324	N74F32DT	1	
U 13	✗ IC,LSTTL,QUAD 2 INPUT OR GATE,SOIC	740878	18324	N74LS32D	1	
U 14, 15	✗ IC,LSTTL,OCTL LINE DRVR,SOIC	742122	18324	N74LS244DT	2	
U 16	✗ IC,FTTL,DUAL 4-1 LINE MUX,SOIC	772806	18324	74F153D	1	
U 17	✗ IC,LSTTL,QUAD D F/F,+EDG TRG,SOIC	742619	01295	SN74LS175ADR	1	
U 18	✗ IC,STTL,600 GATE ARY,9100A-99100,PLCC	741546	61271	MB113T306	1	
U 19	✗ IC,STTL,600 GATE ARY,9100A-99101,PLCC	741553	61271	MB113T306	1	
U 20, 23	✗ IC,BIPOLAR,8-BIT DAC,UP-COMPATIBLE	854158	24355	AD558JP-REEL	2	
U 21, 22	✗ IC,LSTTL,8-BIT BINARY CNTR W/REG,SOIC	782243	01295	SN74LS590DR	2	
U 24, 37	✗ IC,COMPARATOR,QUAD,14 PIN,SOIC	741561	18324	LN339DT	2	
U 25	✗ IC,LSTTL,QUAD BUS,SOIC	740977	18324	N74LS125ADT	1	
U 26, 32, 33	✗ IC,LSTTL, 4 BIT UP/DOWN CNTR,SOIC	742114	18324	N74LS191DT	3	
U 27	✗ IC,LSTTL,DUAL D F/F,+EDG TRG,SOIC	740985	18324	N74LS74ADT	1	
U 28, 29	✗ IC,ECL,QUAD ECL-TTL TRANSLATOR,PLCC	852140	04713	MC10H125FN	2	
U 30	✗ IC,COMPRTR,DUAL,HI-SPEED,16 PIN DIP	782219	6U095	AM687ADL	1	
U 31	✗ IC,FTTL,QUAD D F/F,+EDG TRG,SOIC	801399	18324	74F175DT	1	
U 34	✗ IC,FTTL,4 BIT UP/DOWN COUNTER	854138	07263	74F191SCX	1	
U 35, 36, 39	✗ IC,LSTTL,OCTL BUS TRNSCVR W/3-ST,SOIC	781195	01295	SN74LS245DW	3	
U 38	✗ IC,FTTL,DUAL 4 INPUT NAND GATE,SOIC	742155	18324	N74F20DT	1	
U 40	✗ IC,VOLT REG,FIXED,+5 VOLTS,0.1 AMPS	429910	04713	MC78L05ACP	1	
U 41	✗ IC,OP AMP,QUAD,LOW POWER,SOIC	742569	18324	LM324D	1	
U 42	✗ PROGRAMMED PAL, PROBE-I/O ECL	889704	89536	889704	1	
NOTES:	✗ Static sensitive part.					

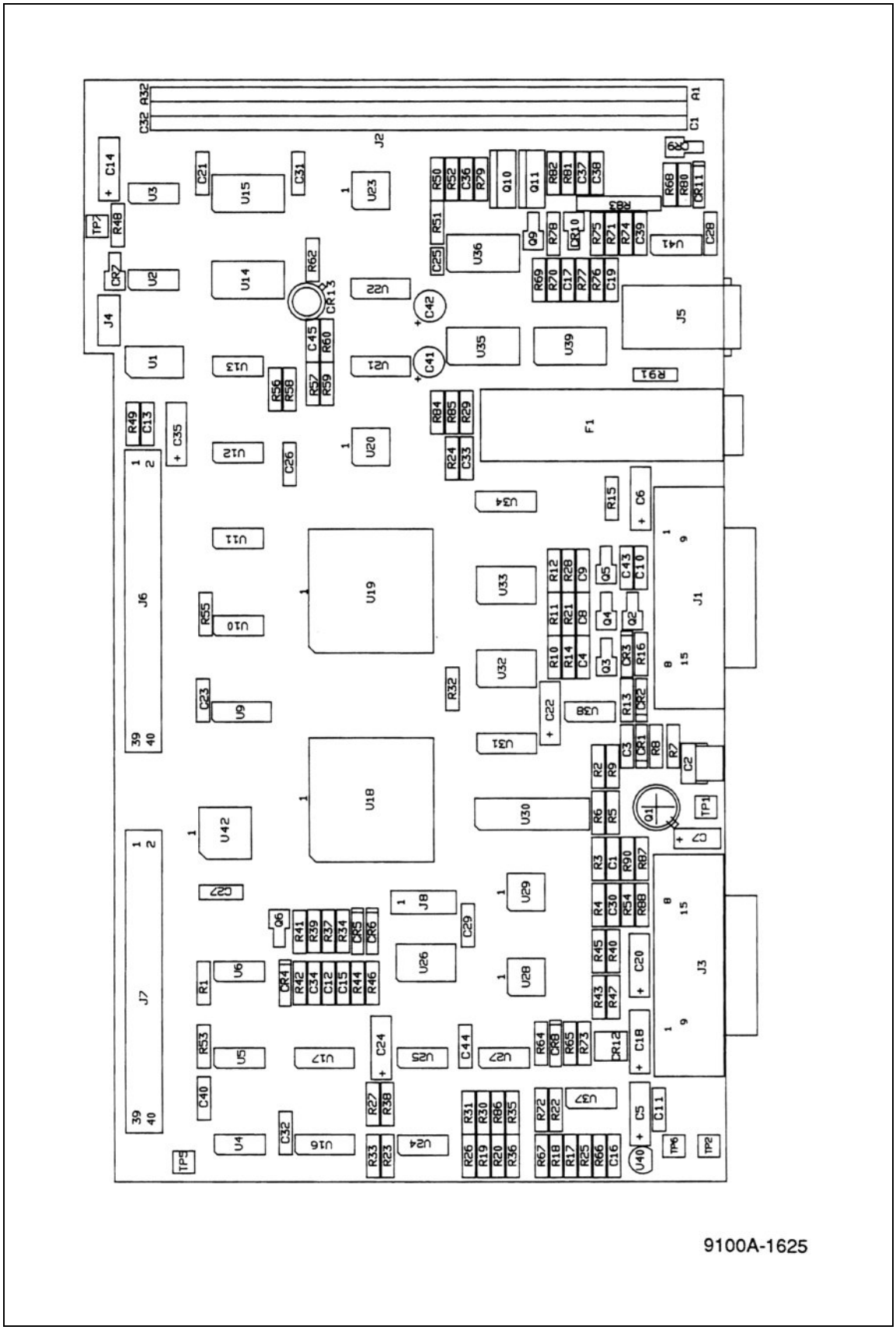


Figure 5-12. A25 Probe I/O-ECL PCA

Table 5-17. Option -003 Parallel I/O Module

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
A 7	↯ I/O MODULE MAIN PCA	768838	89536	768838	1	
A 8	↯ I/O MODULE (TOP) PCA	755611	89536	755611	1	
A 14	CALIBRATION MODULE	813980	89536	813980	1	
A 15	FLYING LEAD MODULE, 20 LEAD SET, TSTD	818708	89536	818708	1	
F 1	FUSE,5X20MM,1A,250V,SLOW	808055	61935	034.3117	1	
F 2	FUSE,.25X1.25,1A,250V,SLOW	109272	71400	MDL-1	1	
H 1	SCREW,PH,P,SS,6-32,.875	801241		COMMERCIAL	4	
H 2	SCREW,PH,P,SEMS,STL,6-32,.250	178533		COMMERCIAL	9	
MP 1	HLDR PART,FUSE,CAP,l/4X1-1/4	460238	61935	031.1666	1	
MP 3	HLDR PART,FUSE,CAP,5X20MM	461020	61935	031.1663	1	
MP 4	CASE TOP, I/O MODULE	773291	89536	773291	1	
MP 5	CASE BOTTOM, I/O MODULE	773283	89536	773283	1	
MP 6	DECAL, CASE TOP, I/O MODULE	805630	22670	805630	1	
MP 7	DECAL, CASE BOTTOM, I/O MODULE	773382	22670	773382	1	
MP 8	SHIELD, I/O MODULE	775866	89536	775866	1	
MP 9	FOOT, NON-SKID	774000	2K262	774000	4	
MP 10	NAMEPLATE, SERIAL -REAR PANEL-	472795	85480	472795	1	
MP 11	BAG,STATIC SHIELDING,15"X18"	681015	89536	681015	1	
MP 12	BAG,STATIC SHIELDING,4"X6"	680884	89536	680884	1	
MP 13	SHIPPING CARTON, LARGE POD	734046	89536	734046	1	
MP 14	FOAM CUSHION, 9900 POD	640508	89536	640508	2	
W 1	CABLE ASSY,I/O MODULE	853069	89536	853069	1	
W 2	WIRE,SHIELD CONTACT	803122	89536	803122	1	
W 3	CABLE ASSEMBLY, EXTERNAL EVENT	773945	89536	773945	1	
NOTES:	↯ Static sensitive part.					

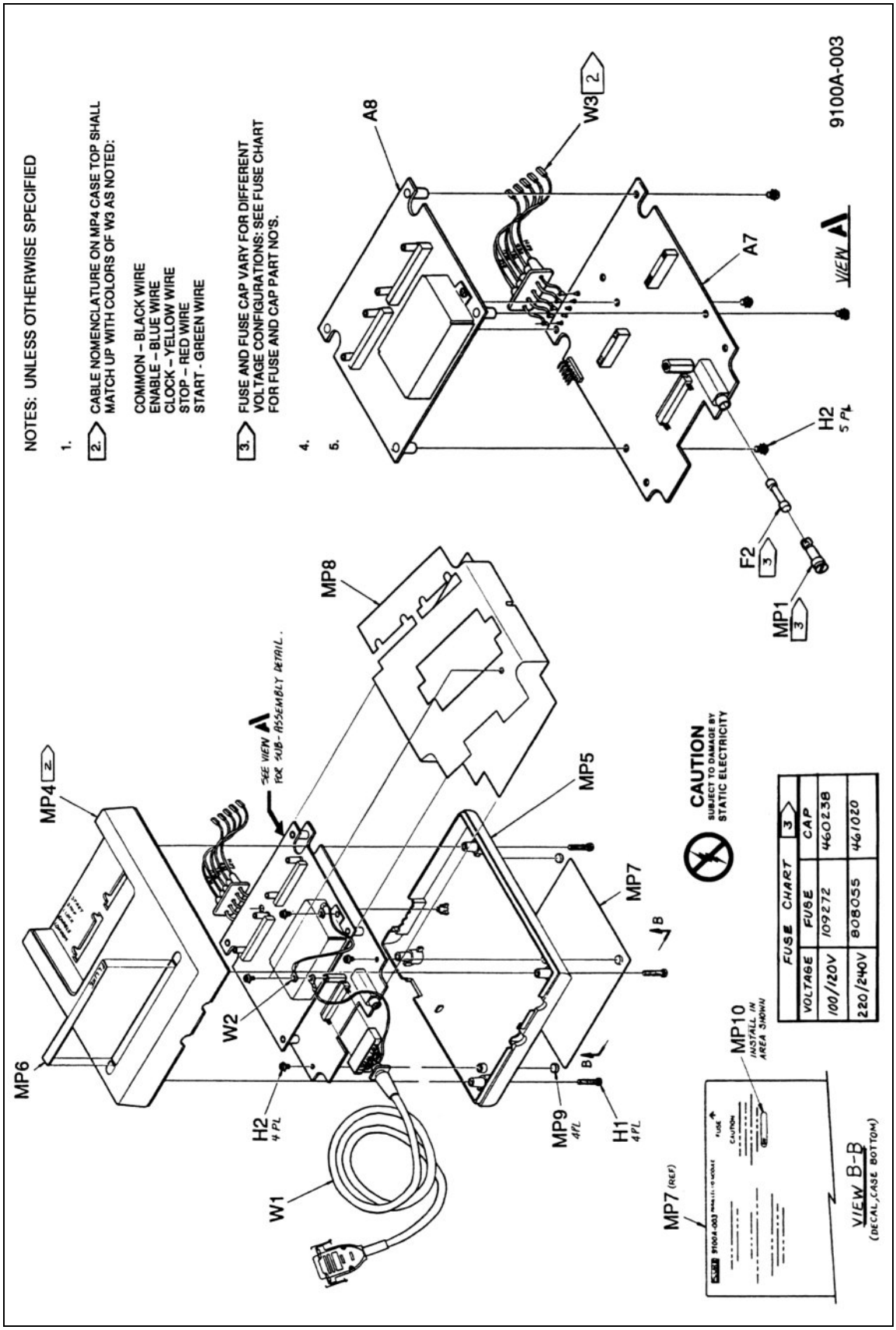


Figure 5-13. -003 Parallel I/O Module

Table 5-18. Option -004 Programmer's Station Monochrome

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
A 4	↯ VIDEO CONTROLLER PCA	768762	89536	768762	1	
A 19	MONOCHROME MONITOR	826362	89536	826362	1	
A 103	KEYBOARD,ASCII FORMAT,ASYNC. SERIAL	887216	51181	E04008051	1	
H 1	RIVET,POP,DOME,AL,0.125X0.316	423616	1B715	AD42AH	2	
MP 1	NAMEPLATE	787275	22670	787275	1	
MP 2	LABEL, COPYRIGHT-86	749887	89536	749887	1	
MP 3	VIDEO CONNECTOR BRACKET	768648	89536	768648	1	
MP 4	NAMEPLATE, SERIAL -REAR PANEL-	472795	85480	472795	1	
MP 5	PROG'MD PROGRAMMER'S DISK	873315	89536	873315	1	
MP 6	PROG'MD DEMO/TRAINER DISK, V4.0, SLVD	854112	89536	854112	1	
MP 7	CARTON KEYBOARD, I/O	805804	89536	805804	1	
MP 8	FOAM INSERT,SHIPPING CONTAINER	870162	89536	870162	3	
MP 9	FOAM PAD, POD SHIPPING CONTAINER	605386	89536	605386	1	
TM 1	9100A PROGRAMMERS MANUAL	813857	89536	813857	1	
U 5	↯ PROGRAMMED 27128-150 v2.0	818195	89536	818195	1	
W 1	CABLE ASSY, MONITOR	870084	89536	870084	1	
Z 1	JUMPER,DIP,0.300CTR,PROGRAM, 8 POS	783183	51167	16-680-191T	1	
NOTES:	↯ Static sensitive part.					

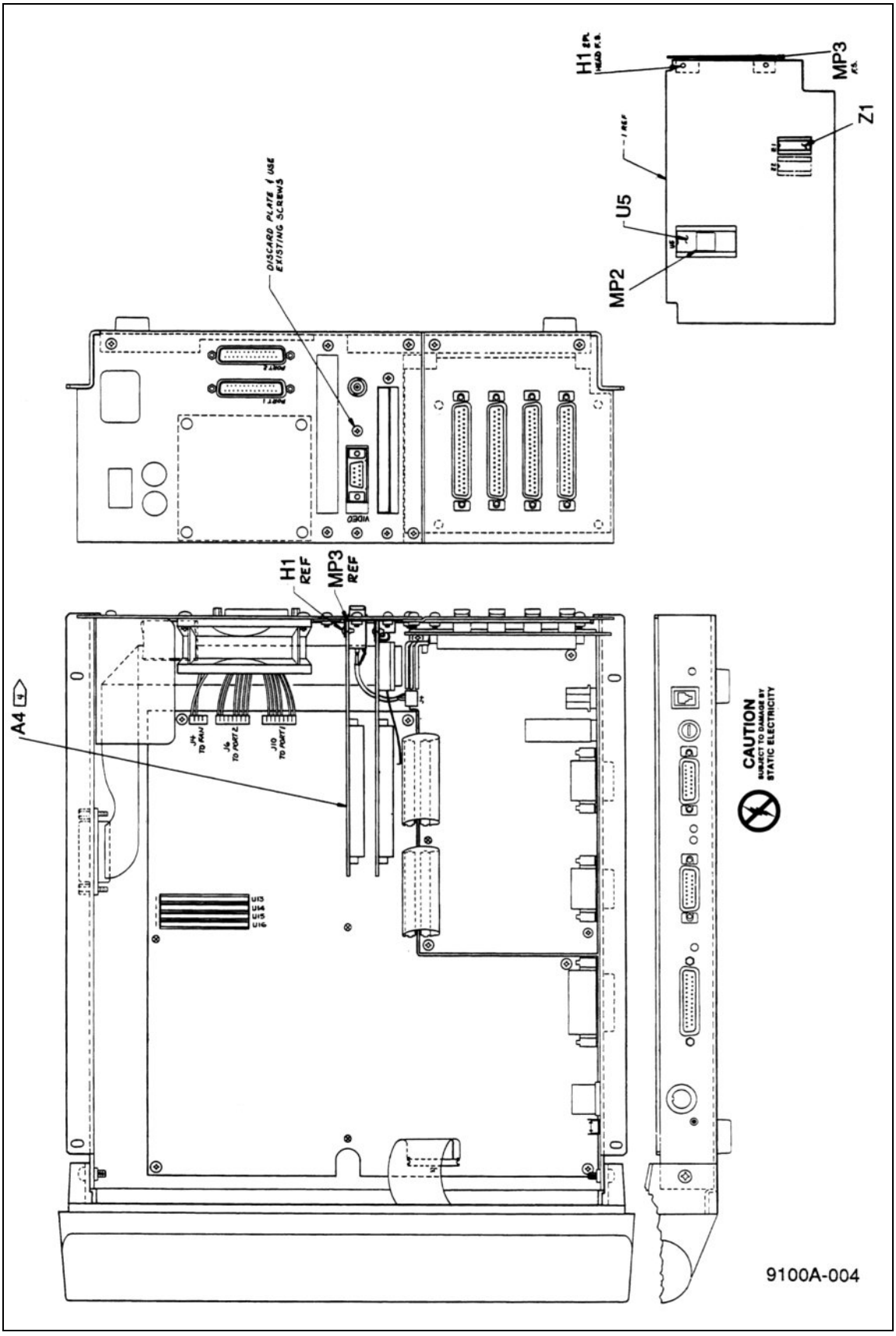


Figure 5-14. -004 Programmer's Station, Mono

Table 5-19. Option -005 Programmer's Station, Color

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
A 4	↯ VIDEO CONTROLLER PCA	768762	89536	768762	1	
A 103	KEYBOARD,ASCII FORMAT,ASYNC. SERIAL	887216	51181	E04008051	1	
H 1	RIVET,POP,DOME,STL,.125X.232	187625	89536	187625	2	
MP 1	NAMEPLATE	787275	22670	787275	1	
MP 2	LABEL, COPYRIGHT-86	749887	89536	749887	1	
MP 4	PROG'MD PROGRAMMER'S DISK	873315	89536	873315	1	
MP 5	PROG'MD DEMO/TRAINER DISKS V4.0, SLVD	854112	89536	854112	1	
MP 6	CARTON KEYBOARD, I/O	805804	89536	805804	1	
MP 7	FOAM INSERT,SHIPPING CONTAINER	870162	89536	870162	3	
MP 8	FOAM PAD, POD SHIPPING CONTAINER	605386	89536	605386	1	
MP 9	VIDEO CONNECTOR BRACKET	768648	89536	768648	1	
TM 1	9100A PROGRAMMERS MANUAL	813857	89536	813857	1	
U 5	↯ PROGRAMMED 27128-150 V2.0	818195	89536	818195	1	
Z 2	JUMPER,DIP,0.300CTR,PROGRAM, 8 POS	783183	51167	16-680-191T	1	
NOTES:	↯ Static sensitive part.					

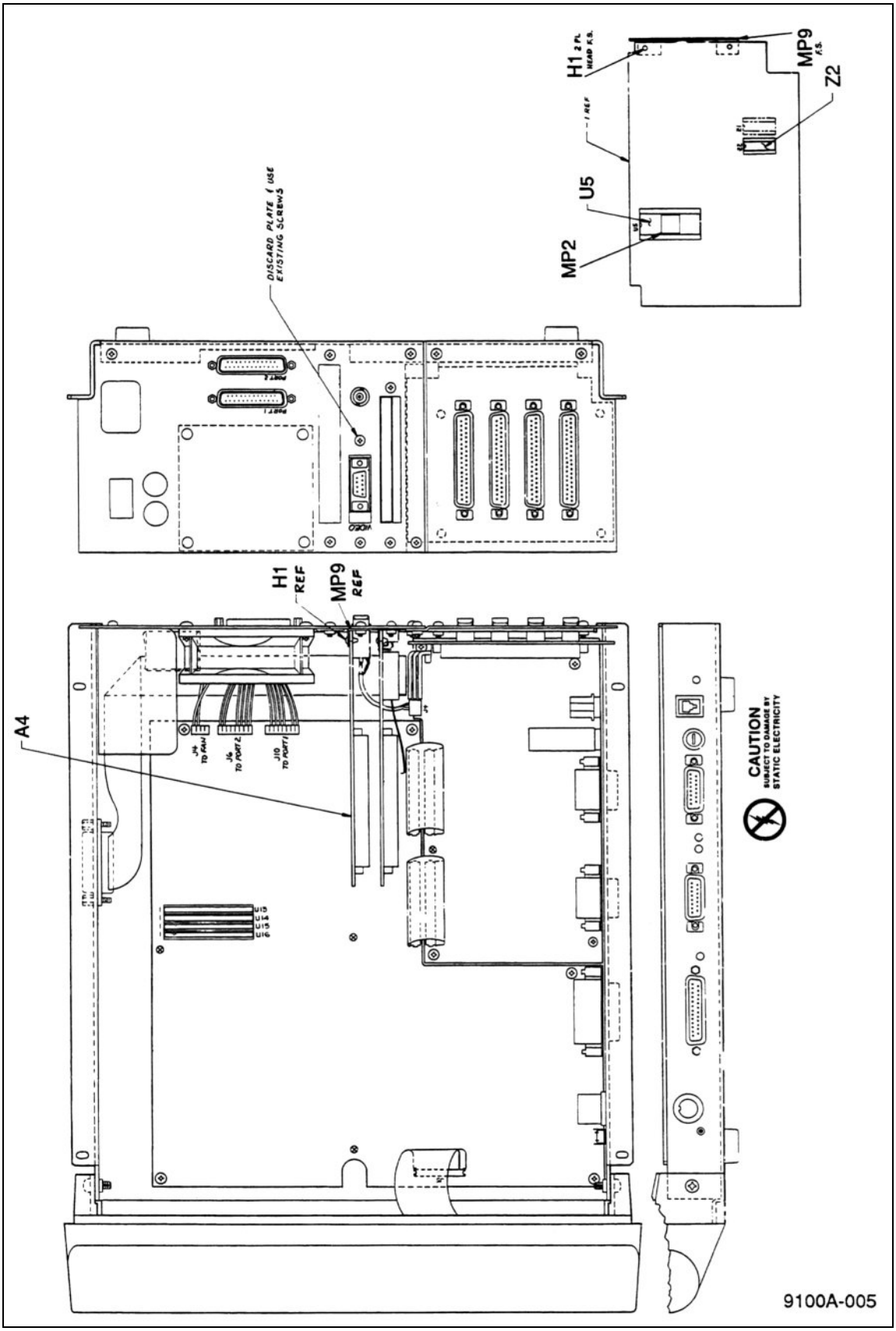


Figure 5-15. -005 Programmer's Station, Color

Table 5-20. Option -009 Video, Monochrome

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
A 4	↯ VIDEO CONTROLLER PCA	768702	89536	768702	1	
A 19	MONOCHROME MONITOR	826362	89536	826362	1	
H 1	RIVET,POP,DOME,AL,0.125X0.316	423616	1B715	AD42AH	2	
MP 1	LABEL, COPYRIGHT-86	749887	89536	749887	1	
MP 2	VIDEO CONNECTOR BRACKET	768648	89536	768648	1	
MP 3	NAMEPLATE, SERIAL -REAR PANEL-	472795	85480	472795	1	
U 5	↯ PROGRAMMED 27128-150 V2.0	818195	89536	818195	1	
W 1	CABLE ASSY, MONITOR	870084	89536	870084	1	
Z 1	BUMPER,DIP,0.300CTR,PROGRAM, 8 POS	783183	51167	16-680-191T	1	
NOTES:	↯ Static sensitive part.					

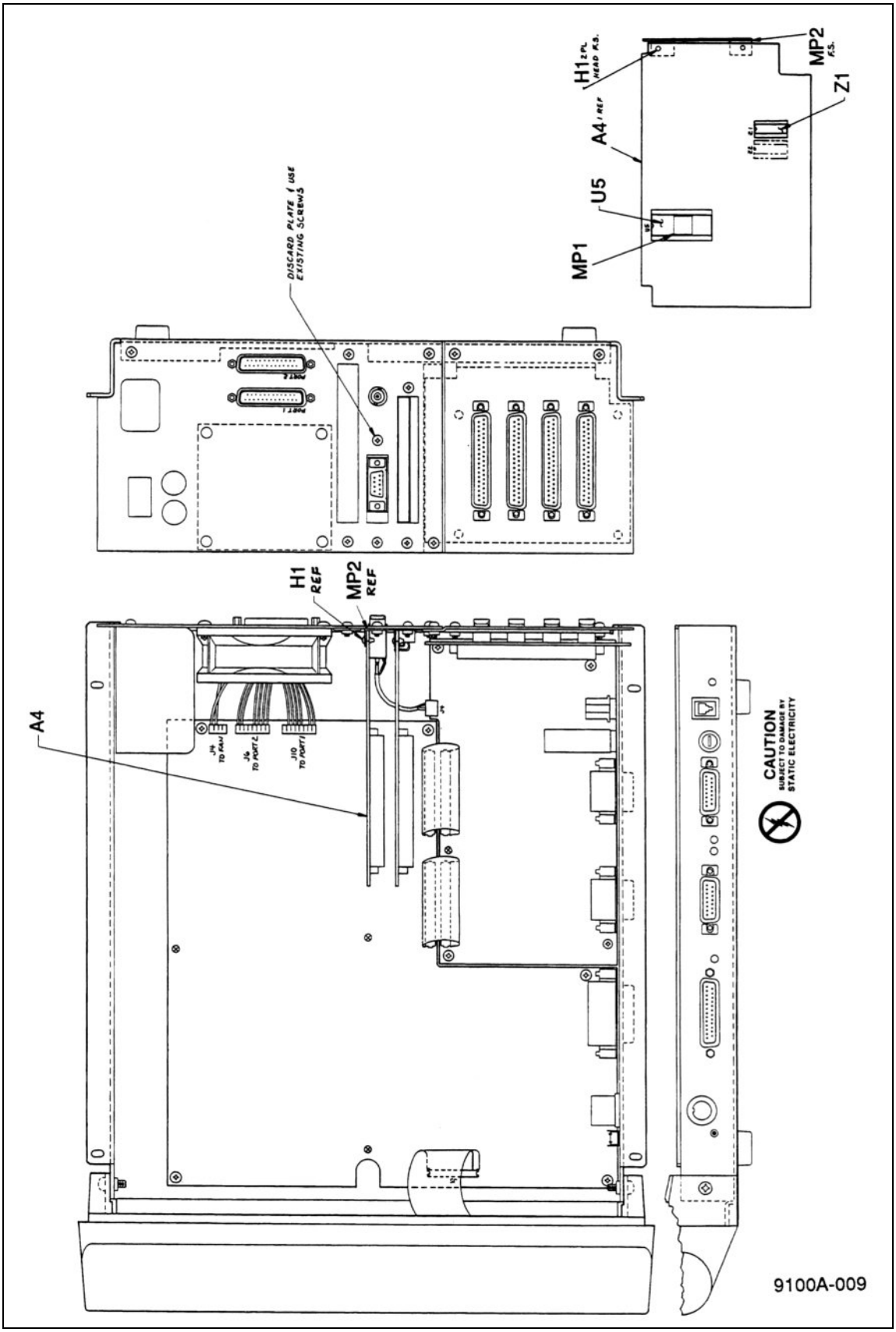


Figure 5-16. -009 Video, Monochrome

Table 5-21. Option -011 Video, Color

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
A 4	↯ VIDEO CONTROLLER PCA	768702	89536	768702	1	
H 1	RIVET,POP,DOME,AL,0.125X0.316	423616	1B715	AD42AH	2	
MP 1	LABEL, COPYRIGHT-86	749887	89536	749887	1	
MP 2	VIDEO CONNECTOR BRACKET	768648	89536	768648	1	
U 5	↯ PROGRAMMED 27128-150 V2.0	818195	89536	818195	1	
Z 2	JUMPER,DIP,0.300CTR,PROGRAM, 8 POS	783183	51167	16-680-191T	1	
NOTES:	↯ Static sensitive part.					

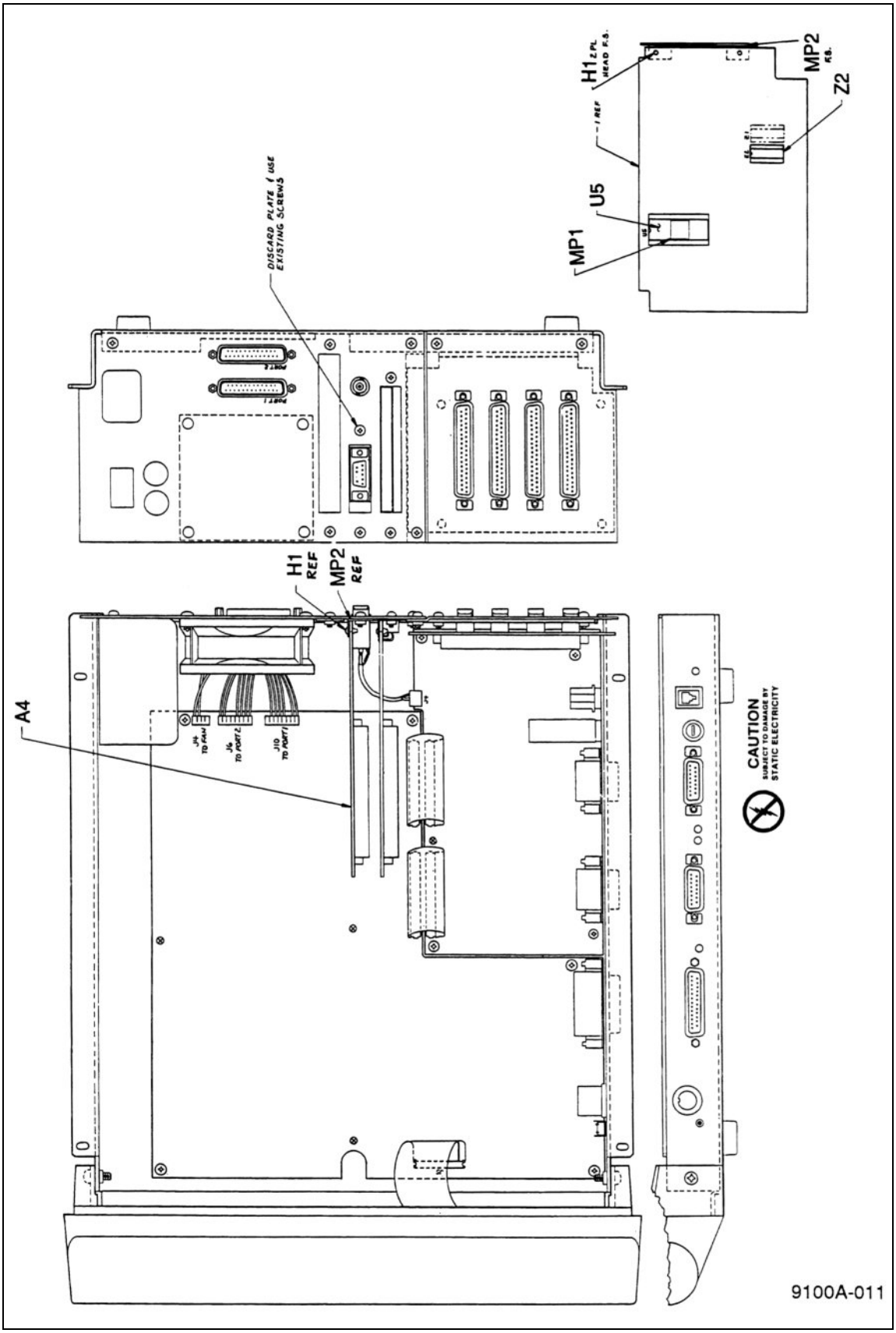


Figure 5-17. -011 Video, Color

Federal Supply Codes for Manufacturers

00779
AMP, Inc.
Harrisburg, PA

01295
Texas Instruments Inc.
Semiconductor Group
Dallas, TX

01537
Champion Technologies Inc.
Formerly Motorola Communications &
Electronics Inc.
Franklin Park, IL

02768
ITW (Illinois Tool Works)
Fastex Division
Des Plaines, IL

04222
AVX Corp.
AVX Ceramics Div.
Myrtle Beach, SC

04713
Motorola Inc.
Semiconductor Products Sector
Phoenix, AZ

05276
ITT Pomona
Electronics Div.
Pomona, CA

06383
Panduit Corp.
Tinley Park, IL

06915
Richco Plastic Co.
Chicago, IL

07047
Ross Milton Co., The
Southampton, PA

07263
Fairchild Semiconductor
North American Sales
Cupertino, CA

08718
ITT Cannon Electric
Phoenix Div.
Phoenix, AZ

0ABX4
Comtec, Inc.
Custer, WA

0B0A9
Dallas Semiconductor corp
Dallas, TX

0BW21
Noritake Co. Inc.
Burlington, MA

0CLN7
Emhart Fastening Group
Shelton, CT

0JTT6
Sony Corp of America
Sony Video Products
Cypress, CA

0K392
Shin-Etsu Silicones of America
(S P America)
Torrance, CA

0KAW4
Conner Peripherals
San Jose, CA

12040
National Semiconductor Corp.
Danbury, CT

15238
ITT Semiconductors
A Div. of International Telephone
& Telegraph Corp.
Lawrence, MA

17856
Siliconix Inc.
Santa Clara, CA
18310

Concord Electronics Corp.
New York, NY

18324
Signetics Corp.
Military Products Div.
Orem, UT

19451
Perine Machinery & Supply Co.
Kent, WA

1B715
Nylok Fastener Corp.
Paramus, NJ

1EX28
Microdisc Services
Bellvue, WA

1M331
E-A-R Div Cabot Corp.
Indianapolis, IN

20584
Enochs Inc.
Indianapolis, IN

21845
Solitron Devices Inc.
Semiconductor Group
Rivera Beach, FL

22526
DuPont, El DeNemours & Co. Inc.
DuPont Electronic Dept.
New Cumberland, PA

22670
GM Nameplate, Inc.
Seattle, WA

23237
IRC, Inc.
Microcircuits Div
Philadelphia, PA

24355
Analog Devices Inc.
Norwood, MA

25088
Siemens Corp.
Iselin, NJ

27014
National Semiconductor Corp.
Santa Clara, CA

27918
Component Parts Corp.
Bellmore, NY

28213
Minnesota Mining & Mfg. Co.
Consumer Specialties Div.
3M Center
Saint Paul, MN

28406
Vaupell Industrial Plastics, Inc.
Seattle, WA

28480
Hewlett-Packard Co.
Corporate HQ
Palo Alto, CA

Federal Supply Codes for Manufacturers (cont)

2K262
Boyd Corp.
Portland, OR

30161
Aavid Engineering Inc.
Laconia, NH

32559
Bivar, Inc.
Irvine, CA

34371
Harris Corp.
Harris Semiconductor
Products Group
Melbourne, FL

44648
Samsung Semiconductor
Inc.
San Clara, CA

4N072
Sheller-Globe
Toledo, Ohio

50541
Hypertronics Corp.
Hudson, MA

51167
Aries Electronics Inc.
Frenchtown, NJ

51406
Murata Erie, No. America
Inc.
Symrna, GA

51809
NCR Corp (National Cash
Registor)
Systemedia Div.
Miamisburg, Ohio

53848
Standard Microsystems
Corp.
Hauppauge, NY

54492
Cinch Clamp Co., Inc.
Santa Rosa, CA

56289
Sprague Electric Co.
Nashua, NH

56708
Zilog Inc.
Campbell, CA

58361
General Instrument Corp.
Optoelectronics Div.
Palo Alto, CA

59124
KOA-Speer Electronics Inc.
Bradford, PA

60395
Xicor Inc.
Milpitas, CA

61271
Fujitsu Microelectronics Inc
San Jose, CA

61429
Fox Electronics
Fort Myers, FL

61752
IR-ONICS Inc
Warwick, RI

61852
Computer Products Inc.
Boschert Div.
Fremont, CA

61935
Schurter Inc.
Petaluma, CA

61964
Omron Electronics Inc.
Schaumsburg, IL

62440
Dreefs Switch
Waukegan, IL

62643
United Chemi-con Inc.
Rosemont, IL

65786
Cypress Semiconductor Corp.
San Jose, CA

68994
Xilinx, Inc.
San Jose, CA

6U095
AMD Enterprises, Inc.
Roswell, GA

70903
Cooper Belden Electronic
Wire & Cable
Geneva, IL

71400
Bussman
Div. of Cooper Industries
Inc.
St. Louis, MO

73020
Gripco Fastener Div.
Black & Decker Corp.
South Whitley, IN

73445
Amperex Electronic Corp.
Hicksville, NY

73734
Federal Screw Products
Inc.
Chicago, IL

74868
Amphenol Corp.
Danbury, CT

75915
Littelfuse Tracor, Inc.
(Formerly: Tracor-Littelfuse)
Des Plaines, IL

76854
Oak Switch Systems Inc.
Crystal Lake, IL

78189
Illinois Tool Works Inc.
Shakeproof Div.
Elgin, IL

78553
Eaton Corp.
Engineered Fastener Div.
Cleveland, OH

7Z884
ALPS, Inc.
Seattle, WA

83553
Associated Spring Barnes
Group, Inc.
Gardena, CA

85480
W H Brady Co. Corp.
Industrial Products Div
Milwaukee, WI

86928
Seastrom Mfg. Co. Inc.
Glendale, CA

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88245
Winchester Electronics
Litton Systems-Useco Div.
Van Nuys, CA

88690
United Technologies, Inc.
Automotive Products Div.
Dearborn, MI

89536
John Fluke Mfg. Co., Inc.
Everett, WA

8A233
Philips ECG Inc.
Div. of North American
Philips Corp.
Williamsport, PA

91506
Augat, Inc.
Attleboro, MA

91637
Dale Electronics Inc.
Columbus, NE

96652
Medalist Industries
Leitzke Div.
Hustisford, WI

9R216
Data Composition Services,
Inc
Laurel, MD

9W423
Amatom Electronic Hard-
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El Monte, CA

06915
Richco Plastic Co.
Chicago, IL

0DSM7
Conductive (Pkg) Contain-
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TLX: (393) 22085 ESIND

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el. Mohandessin
P.O. Box 242
Dokki Cairo
TEL: 20 2 490922
TLX: 22816 phegy un

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Phillips Scientific
Test & Measuring Division
Colonial Way
Watford
Hertfordshire WD2 4TT
TEL: 44 923-240511
TLX: 851 934583 PHI TMD

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Service VSF
Unternehmensbereich Elektronik fuer Wissenschaft und Industrie
Oskar-Messter-Strasse 18
D-8045 Ismaning
TEL: 49 89 9605 261

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Oy Phillips AB
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P.O. Box 11
02631 ESPOO
TEL: 358 0 52572
TLX: 121875 fixheps

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Science et Industry
105 Rue de Paris BP 62
93002 Bobigny, Cedex
TEL: 33-1-4942-8040
TLX: 210290 induphi

Greece
Phillips S.A. Hellenique
15,25th March Street
177 78 Tavros
10210 Athens
TEL: 30 1 4894911
TLX: 241566/241567frtgraa

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TLX: (780) 76762 SCHMC HX

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Bangalore 560 080
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TLX: (953) 845271 HSPL IN

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Mahal Industrial Estate
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Bombay 400 093
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TLX: (953) 11-79387 HEMC IN

Hindtron Services Pvt. Ltd.
15 Community Centre
Panchshila Park
New Delhi 110 017
TEL: 011-6433675
TLX: (953) 031-61458 HCPL IN

Hinditron Services Pvt. Ltd.
Field Service Center
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5th Floor
114 Sarojini Devi Road
Secunderabad 500 003
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TLX: (953) 425-6973

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TLX: 1171038 FAIRME

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5000 AC Tilburg
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TLX: 52683 FLUKE

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TLX: (952) 24494 PIO PK

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TLX: (394) 25663 PE IREING

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Metro Manila 1502
TEL: 63 2 700-621
TLX: (722) 27901 RLA PH

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I&E Division
Estrada de Outurela-Carnaxide
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TLX: 65120 P1 .PGAJ

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African Phillips (Pty) Ltd.
I&E Service Mgr.
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Rank O'Connor's Singapore Pte
Ltd
98 Pasir Panjang Road
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TEL: 65 4737944
TLX: (786) RS21023 OCONSIN

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Depto. Tecnico Instrumentacion
c/Martinez Villergas 2
28027 Madrid
TEL: 34 1 4042200
TLX: 052-27710 dsxma eesm/op

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Phillips Kistaindustrier AB
I&E Technical Customer Support
Borgarfjordsgatan 16
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TLX: 854 17173 PHILKI S

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Phillips A.G.
Technischer Kundendienst
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Allmendstrasse 140
CH-8027 Zurich
TEL: 41 1 488 29 63
TLX: 815 780 11

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Commercial Building,
344 Min Sheng East Road
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TEL: 886 2 501-3468
TLX: (785) 11111 SCHMIDT

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Measuretronix Ltd.
2102/31 Ramkamhaeng Road
Bangkok 10240
TEL: 66 2 375-2733,375-2734
TLX: (788) 82796 HUAMARK TH

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Inonu Caddesi 78/80
Posta Kutusu 504-Beyoglu
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Libertad 2525
Montevideo
TEL: 598-2-789015
TLX: (398) COAUR UY23010

Venezuela
Coasin C.A.
Calle 9 Con Calle 4, Edif. Edinurbi
Apartado de Correos Nr-70-136
Los Ruices
Caracas 1070-A
TEL: 58 2 241-0309, 241-1248
TLX: (395) 21027 EMVEN VC

Section 6
Schematic Diagrams

NOTE

A12 schematic also used with A15 Flying Lead Module

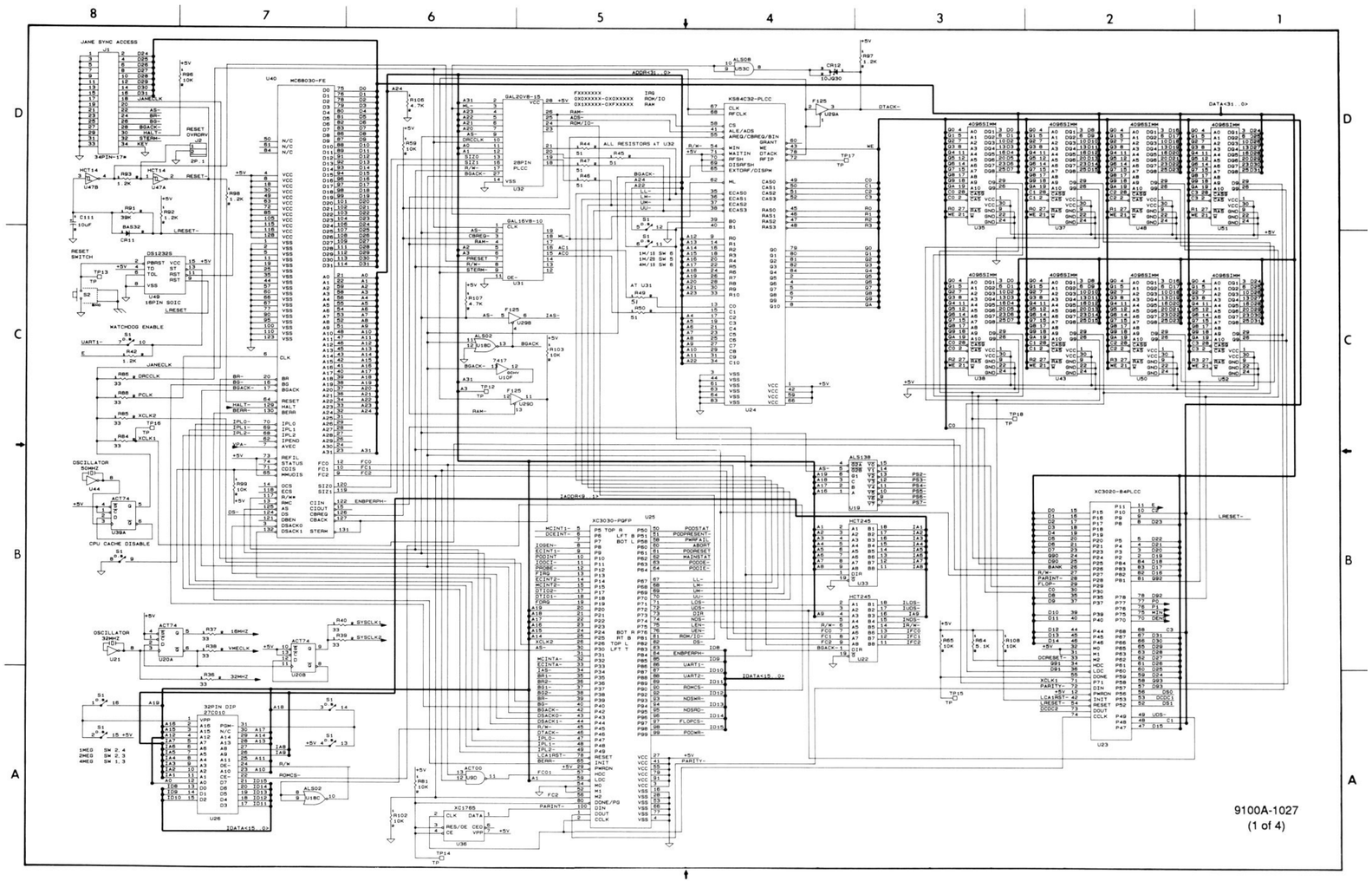


Figure 6-1. A1 Main PCA

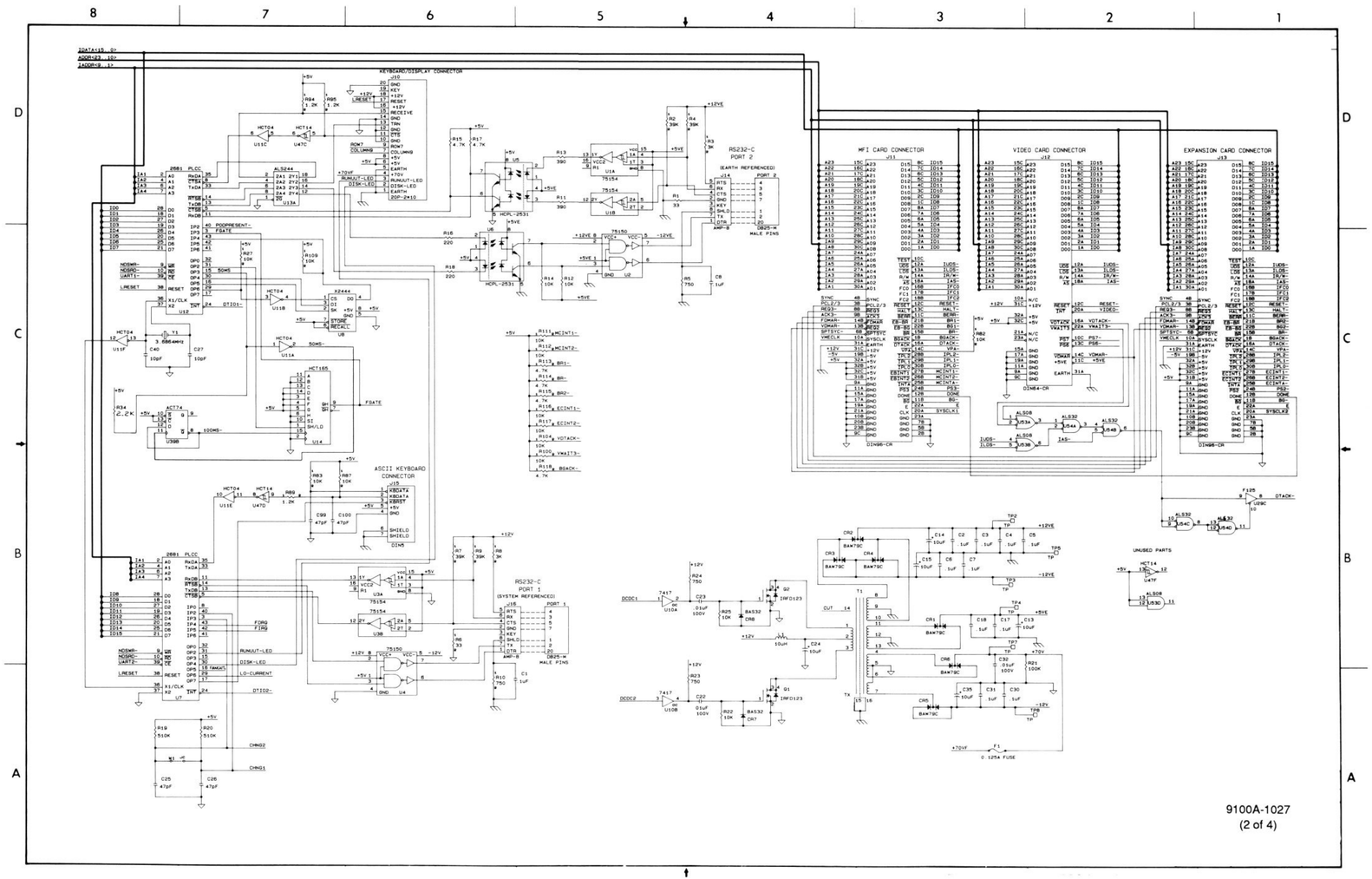


Figure 6-1. A1 Main PCA (cont)

9100A-1627

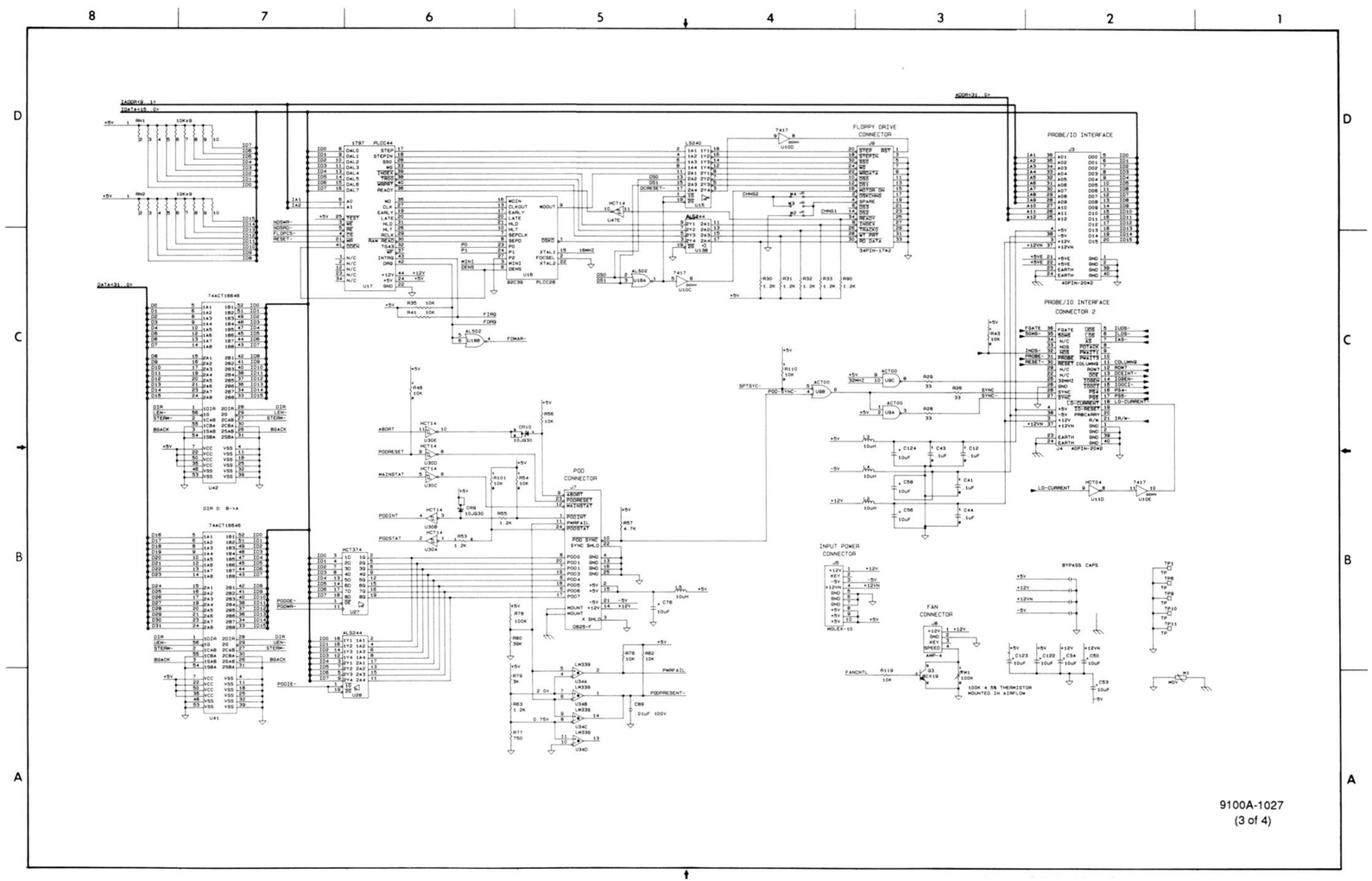


Figure 6-1. A1 Main PCA (cont)

9100A-1627

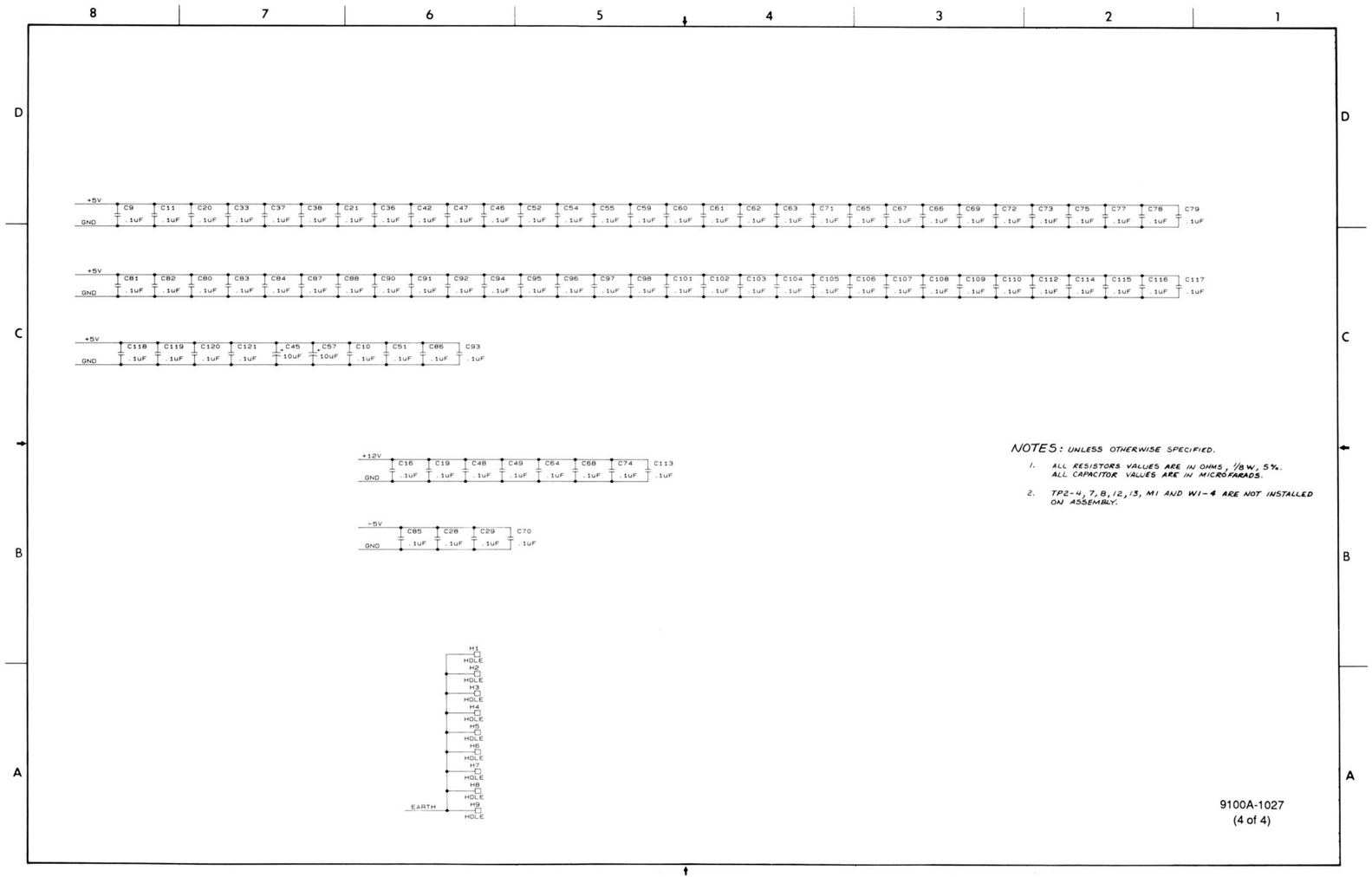
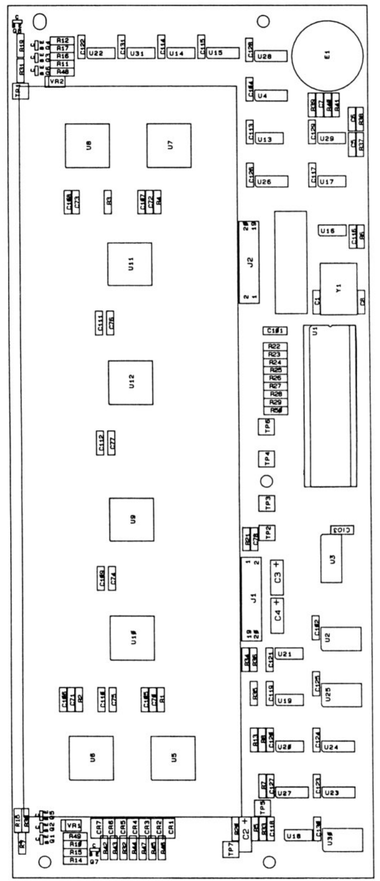


Figure 6-1. A1 Main PCA (cont)



9100A-1602

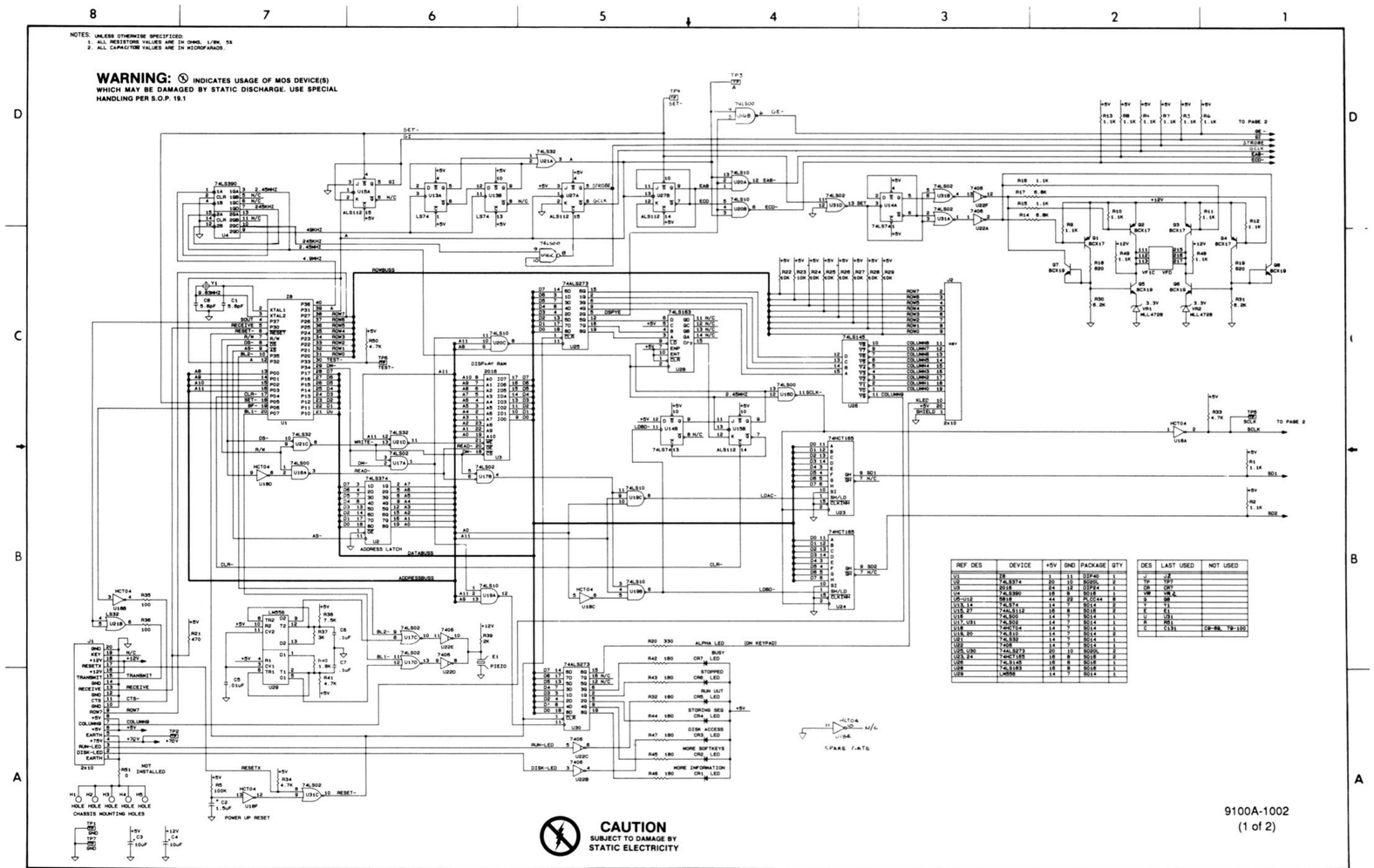
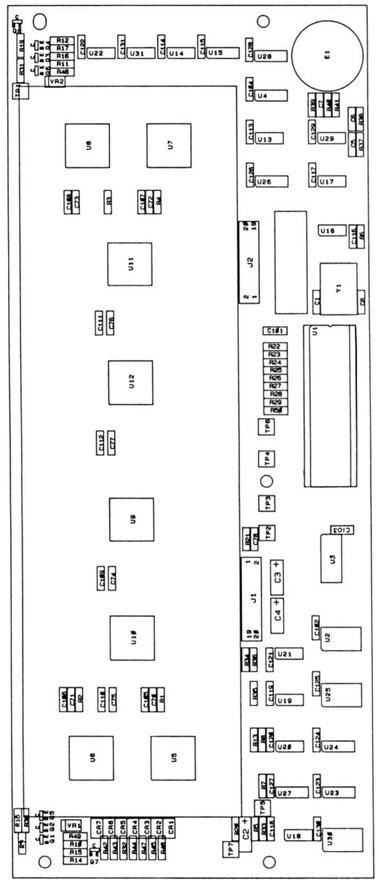


Figure 6-2. A2 Display Interface PCA



9100A-1602

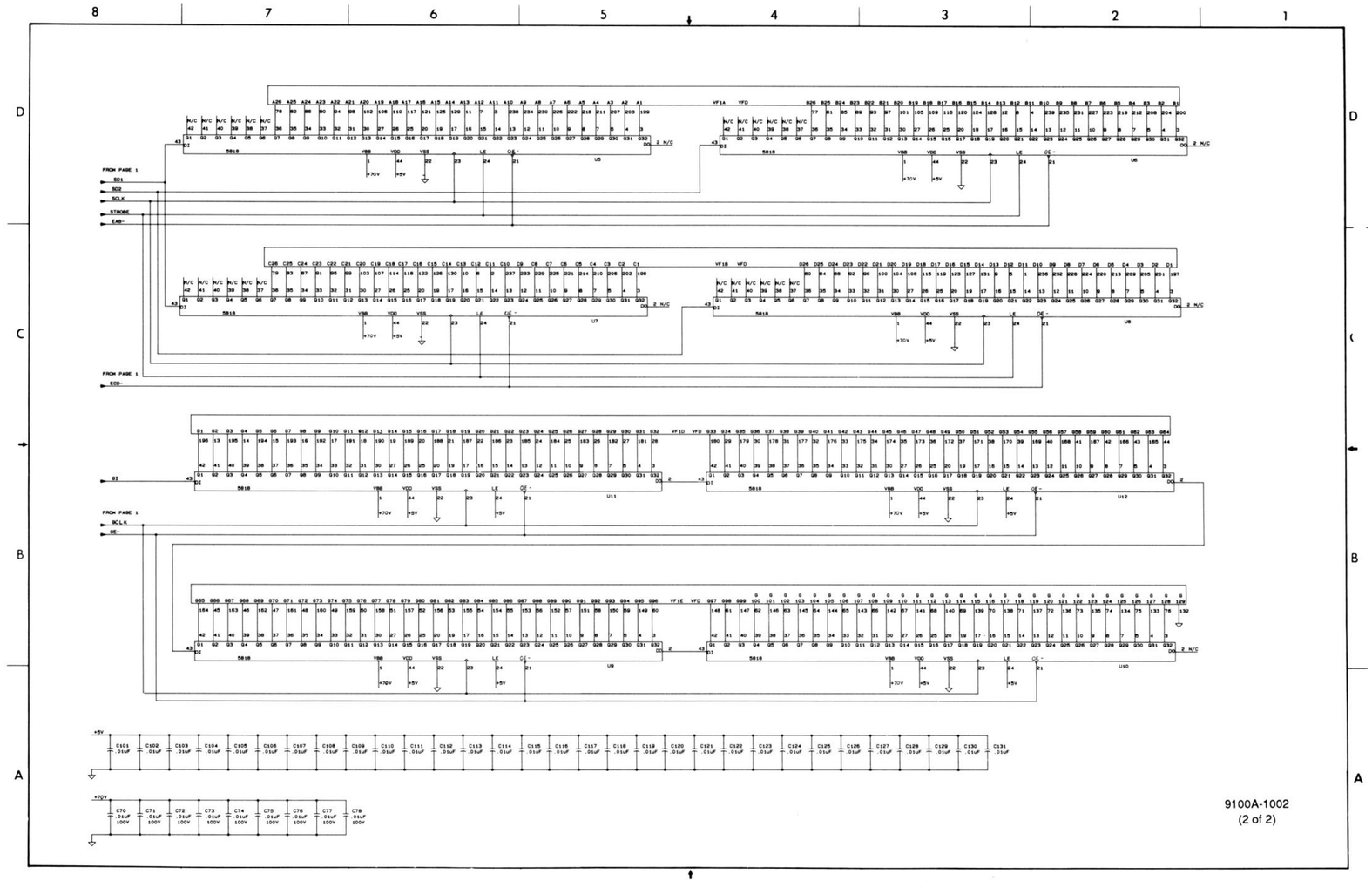
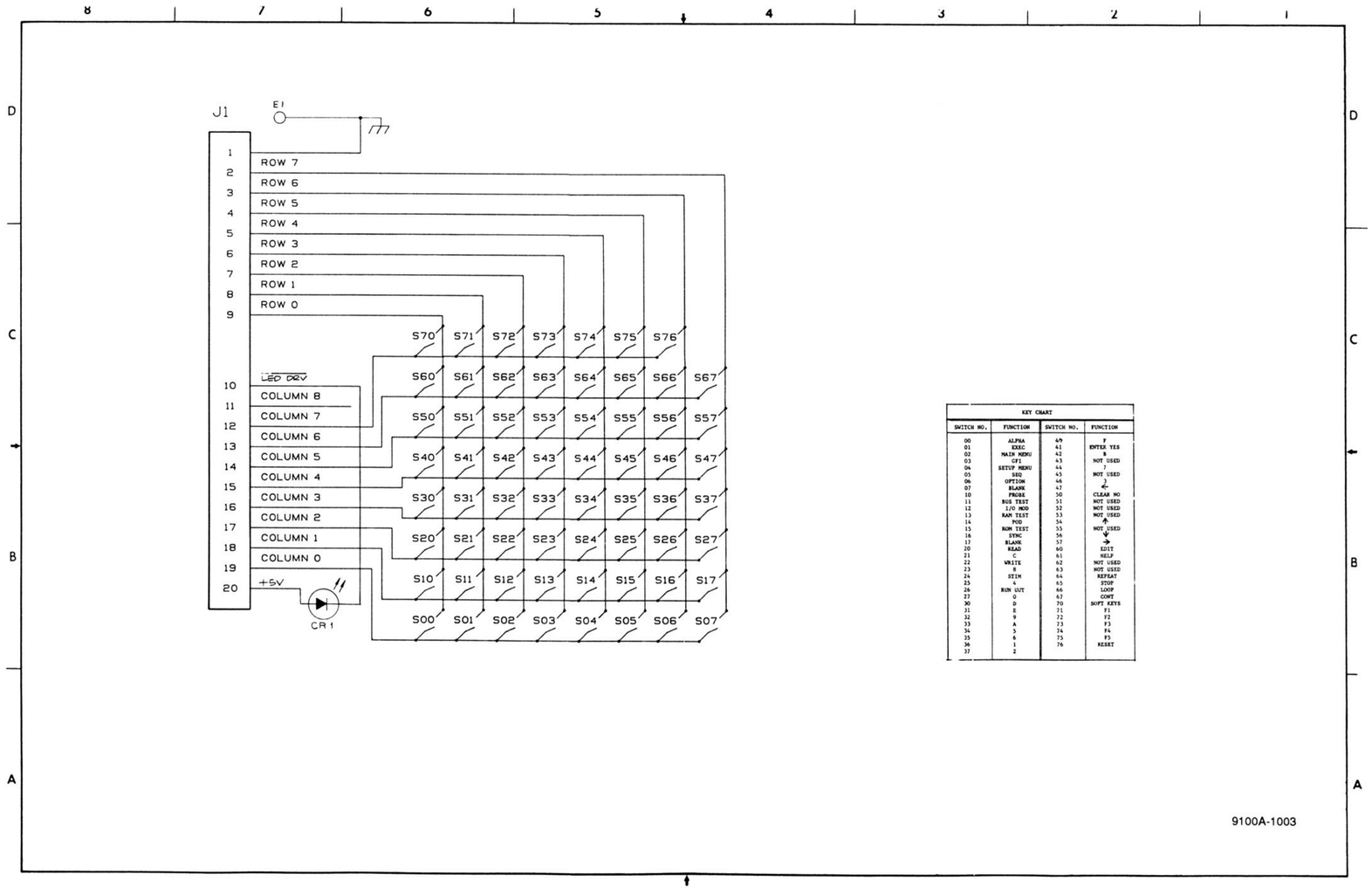


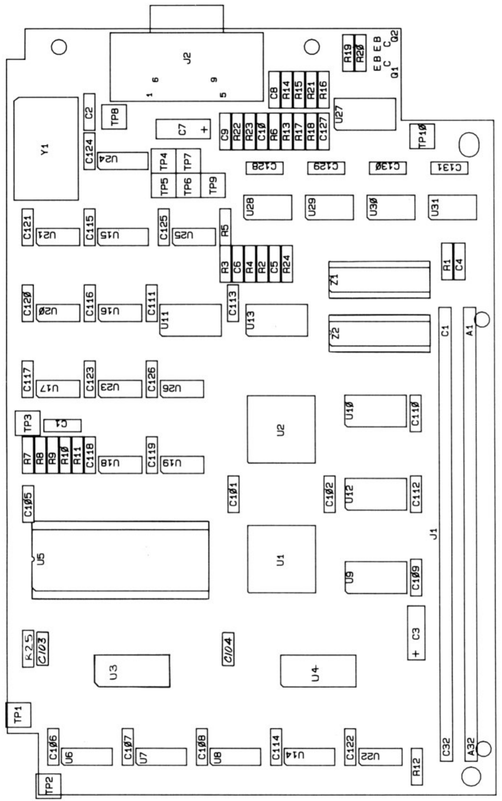
Figure 6-2. A2 Display Interface PCA (cont)



KEY CHART

SWITCH NO.	FUNCTION	SWITCH NO.	FUNCTION
00	ALPHA	40	F
01	EXEC	41	ENTER YES
02	MAIN MENU	42	B
03	GFI	43	NOT USED
04	SETUP MENU	44	7
05	SEQ	45	NOT USED
06	OPTION	46	3
07	BLANK	47	↓
10	PROBE	50	CLEAR NO
11	BUS TEST	51	NOT USED
12	I/O MOD	52	NOT USED
13	RAM TEST	53	NOT USED
14	PUD	54	↑
15	ROM TEST	55	NOT USED
16	SYNC	56	↓
17	BLANK	57	→
20	READ	60	EDIT
21	C	61	HELP
22	WRITE	62	NOT USED
23	R	63	NOT USED
24	STIM	64	REPEAT
25	L	65	STOP
26	RUN UUT	66	LOOP
27	U	67	CONT
30	D	70	SOFT KEYS
31	E	71	F1
32	9	72	F2
33	A	73	F3
34	5	74	F4
35	6	75	F5
36	1	76	RESET
37	2		

Figure 6-3. A3 Keypad PCA



9100A-1604

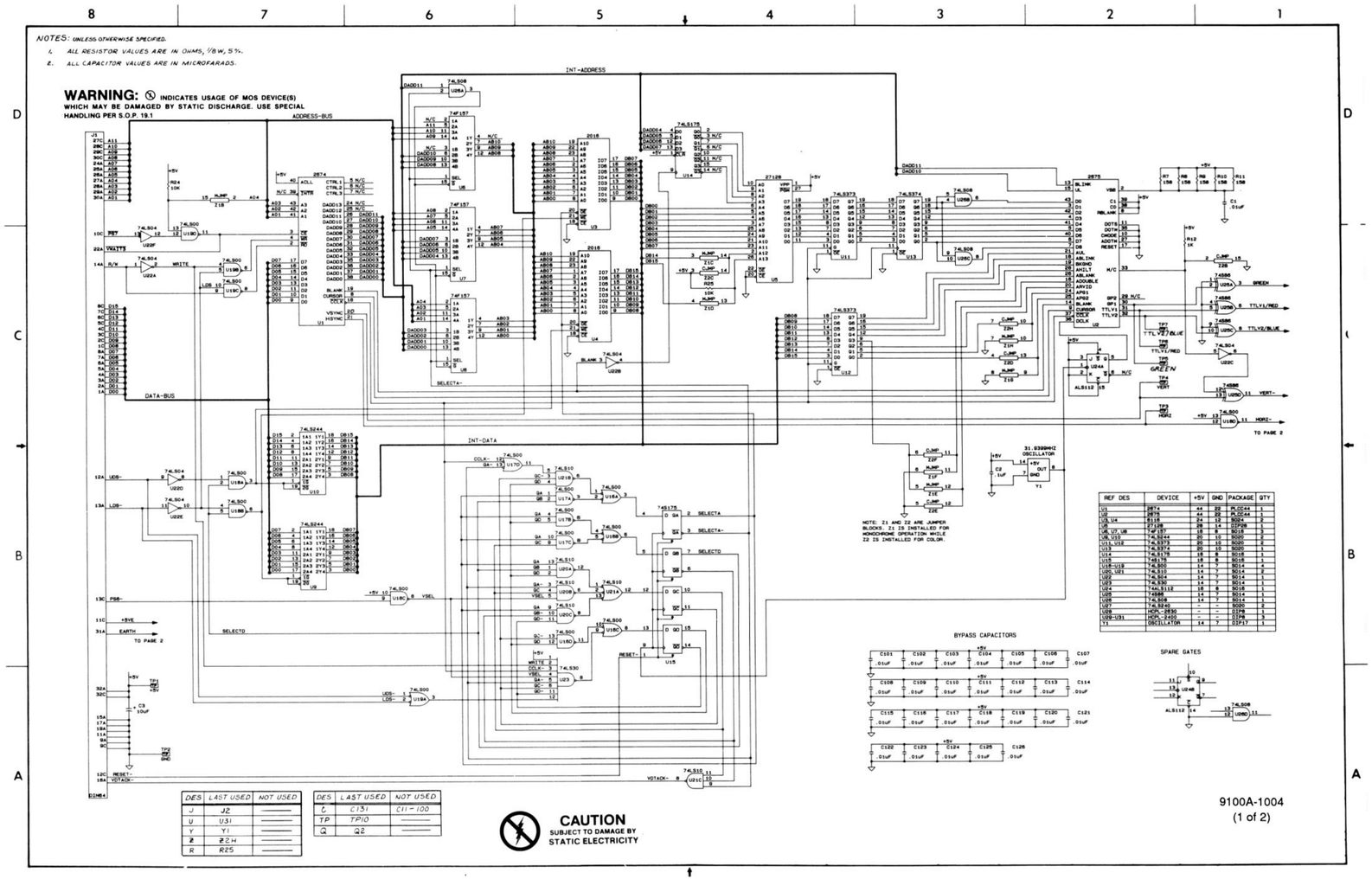
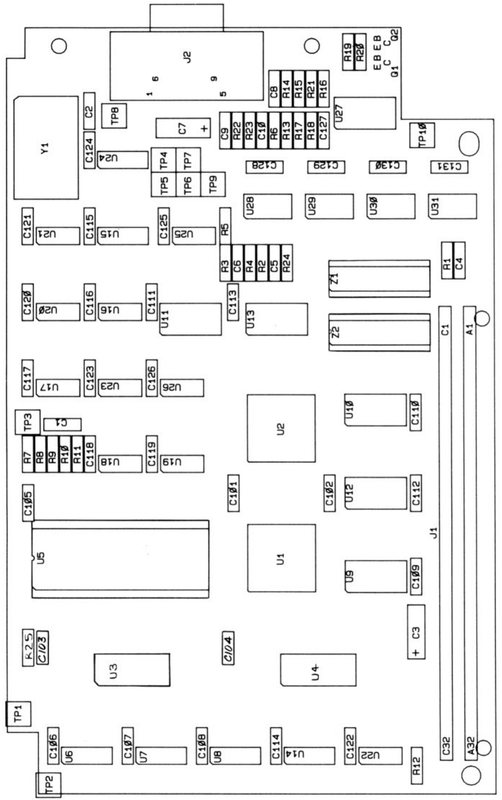


Figure 6-4. A4 Video Controller PCA



9100A-1604

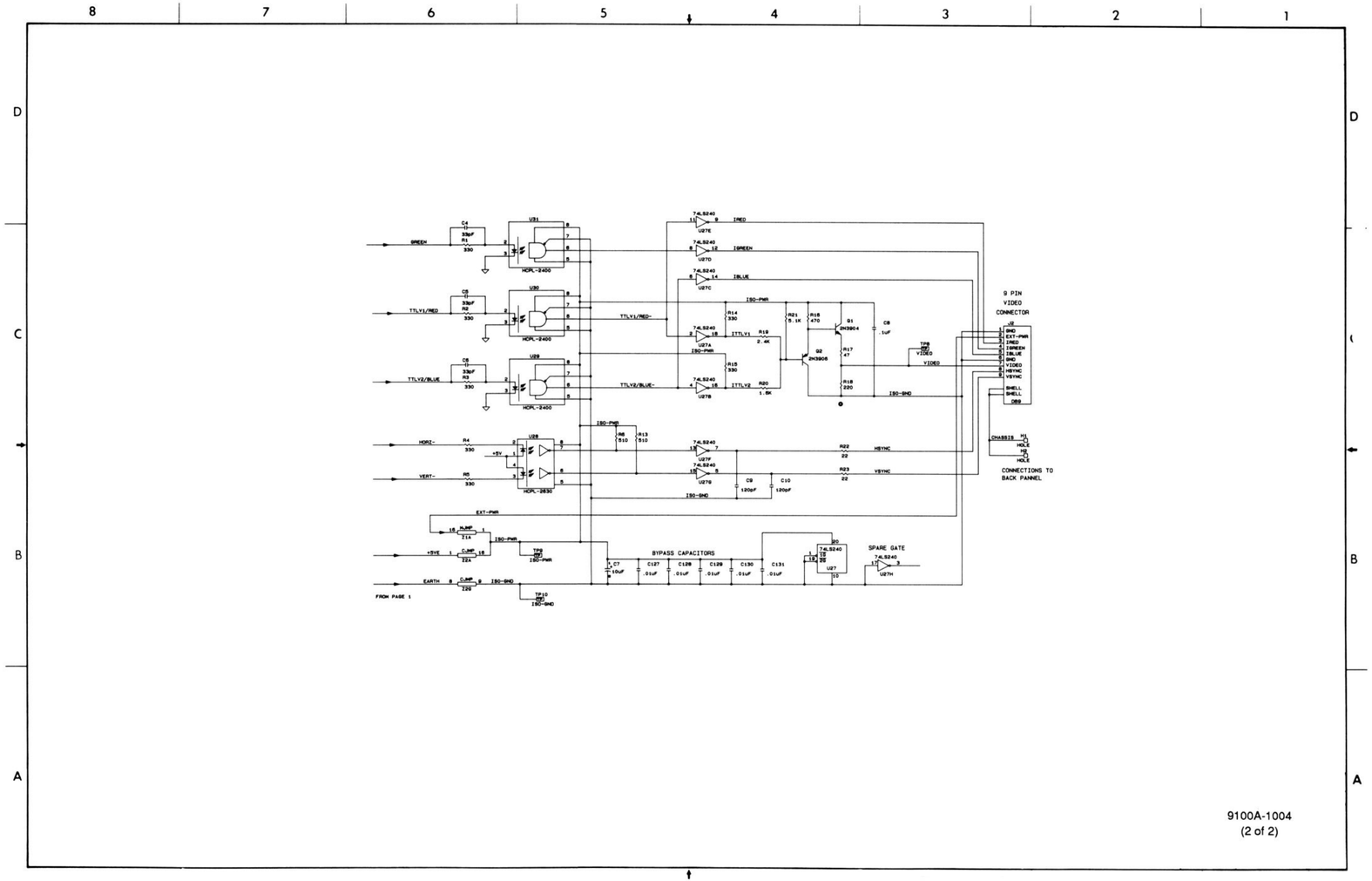
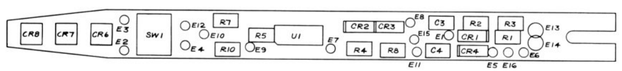


Figure 6-4. A4 Video Controller PCA (cont)

CKT 1



CKT 2

9100A-1605

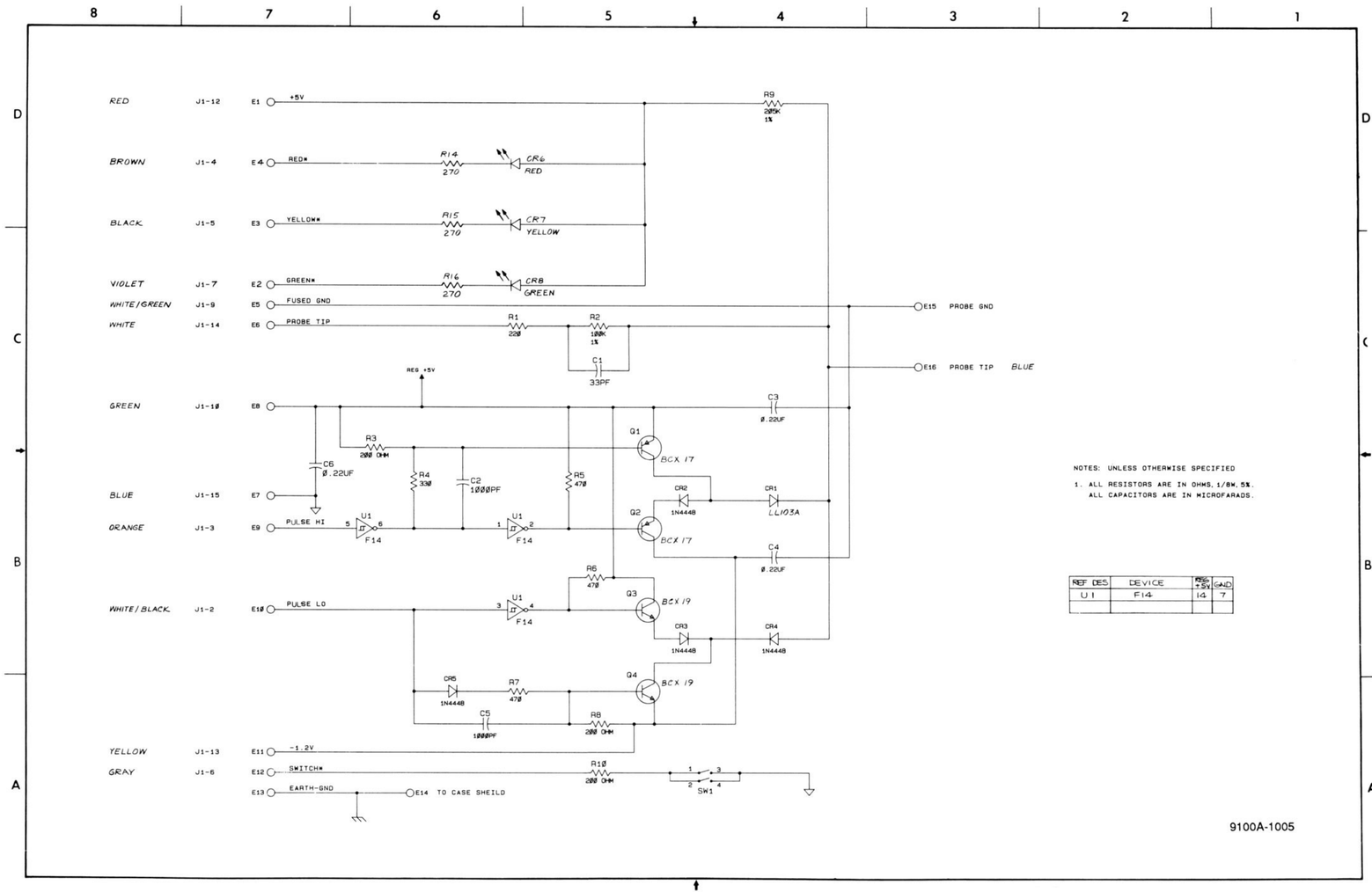
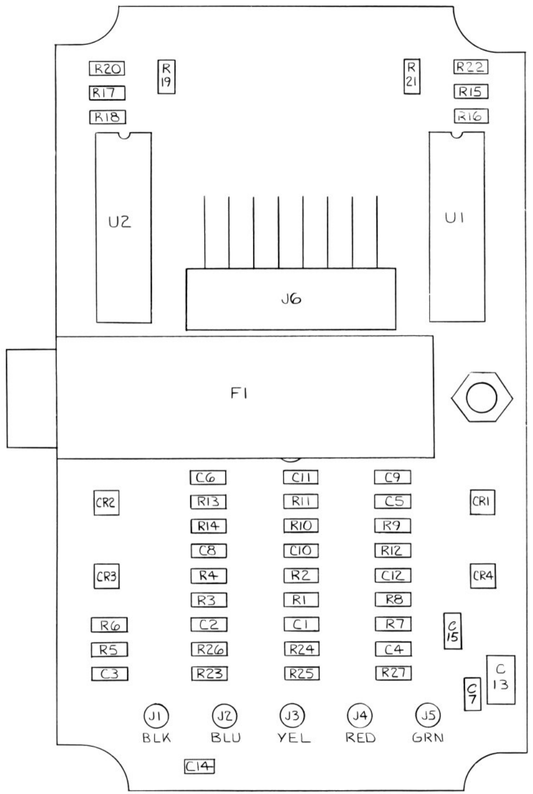


Figure 6-5. A5 Probe PCA



9100A-1606

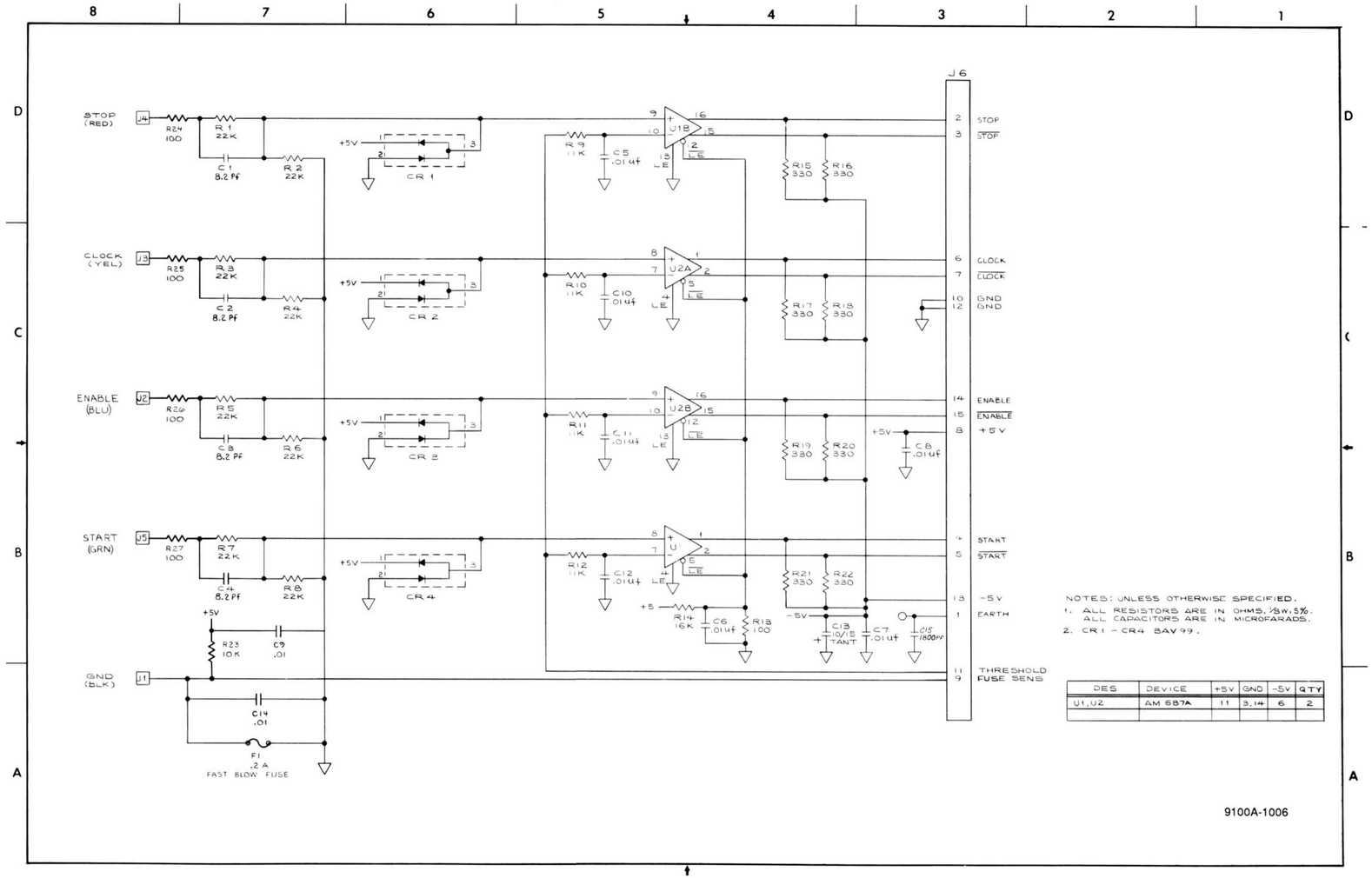
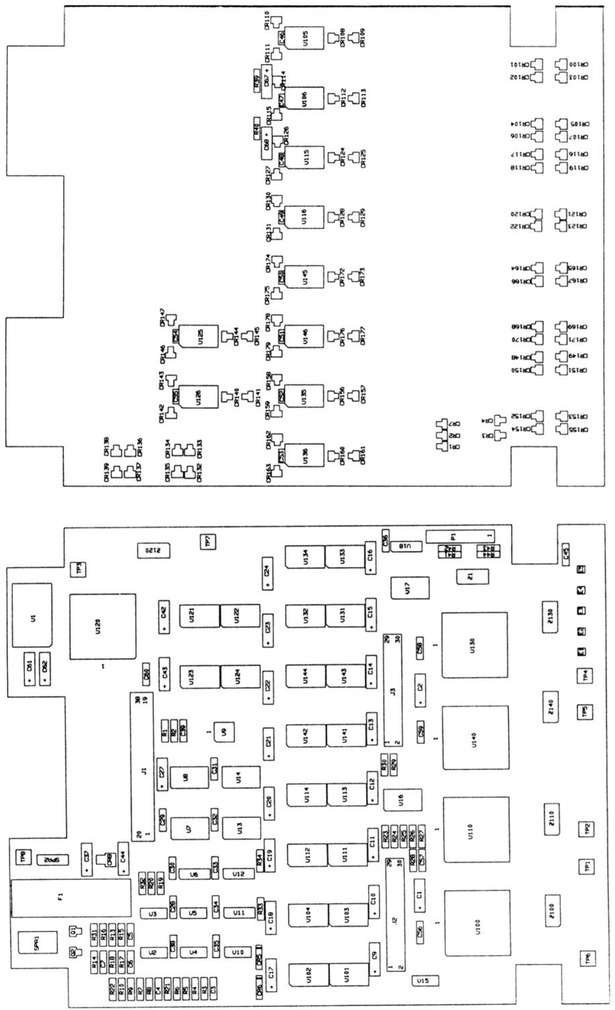


Figure 6-6. A6 Clock Module PCA



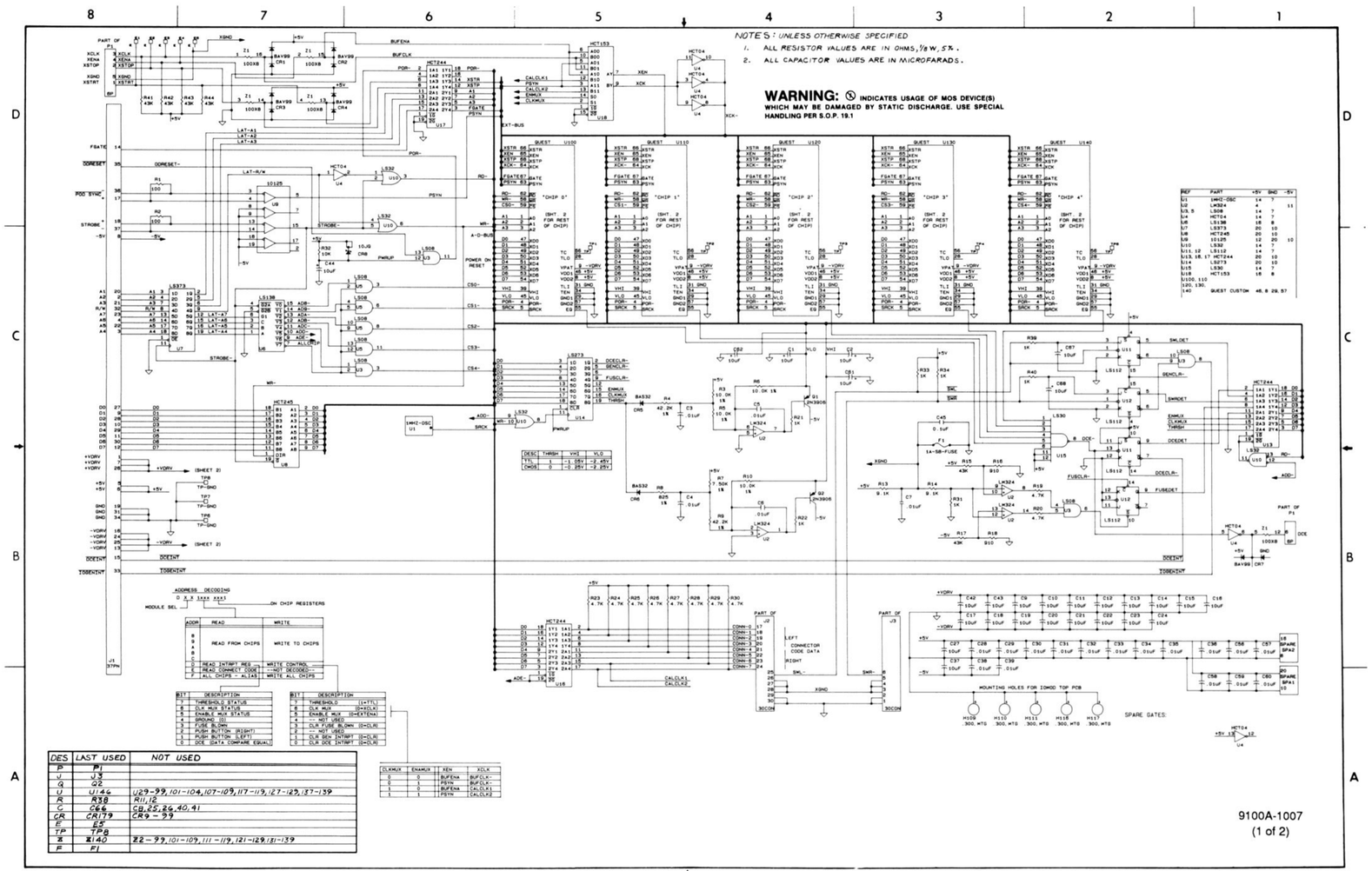
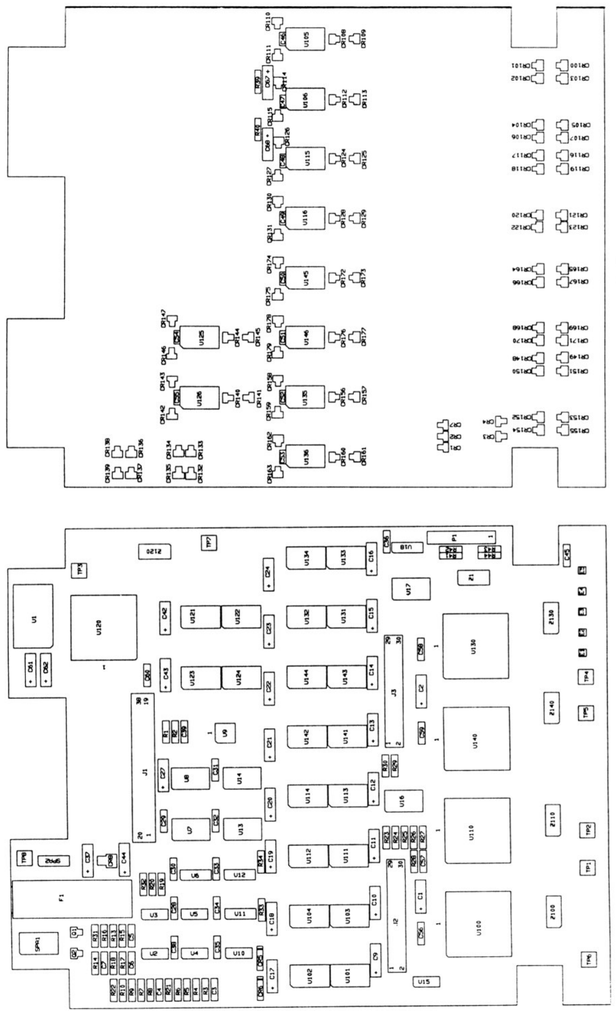


Figure 6-7. A7 I/O Module (Main) PCA



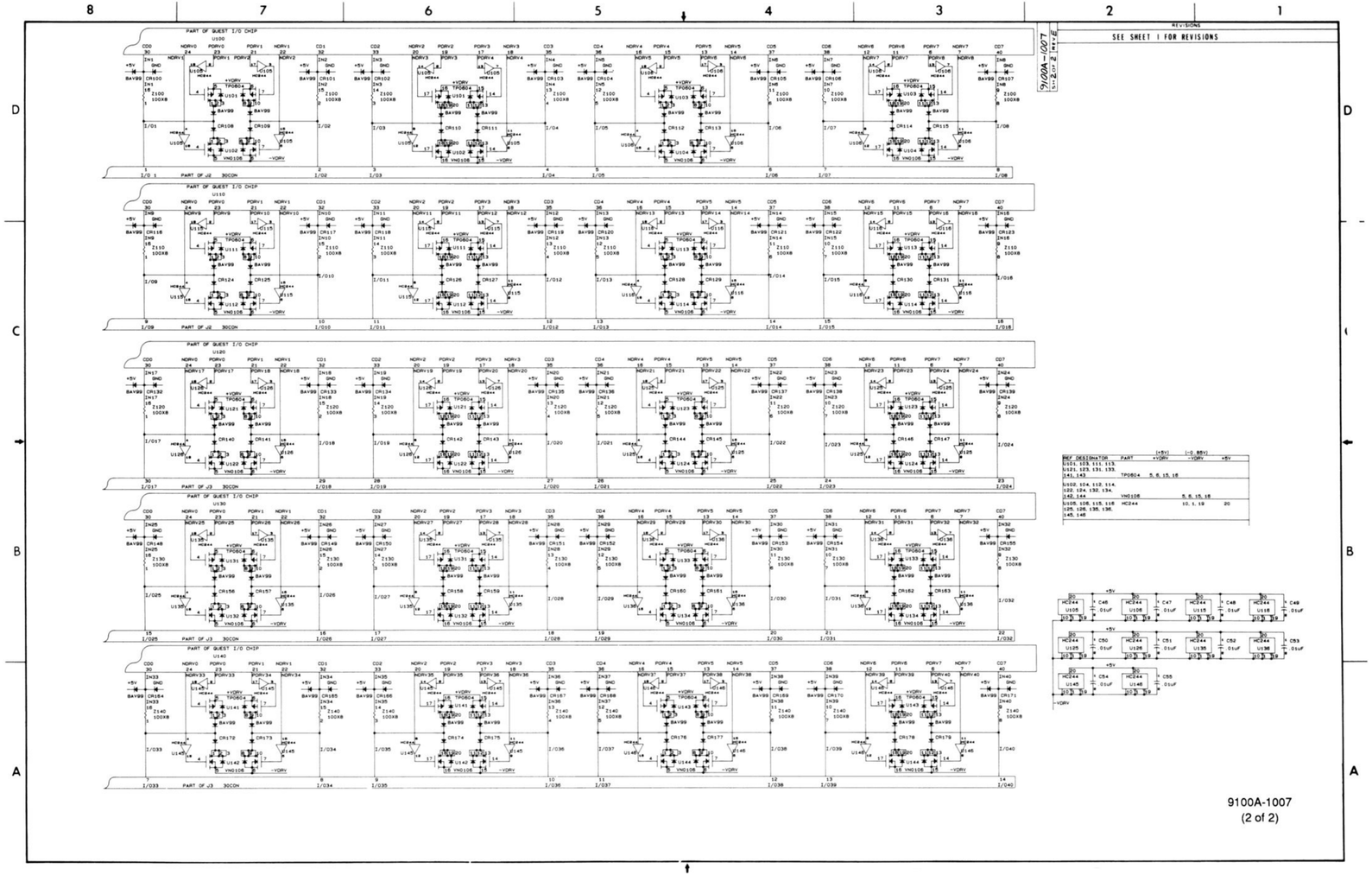
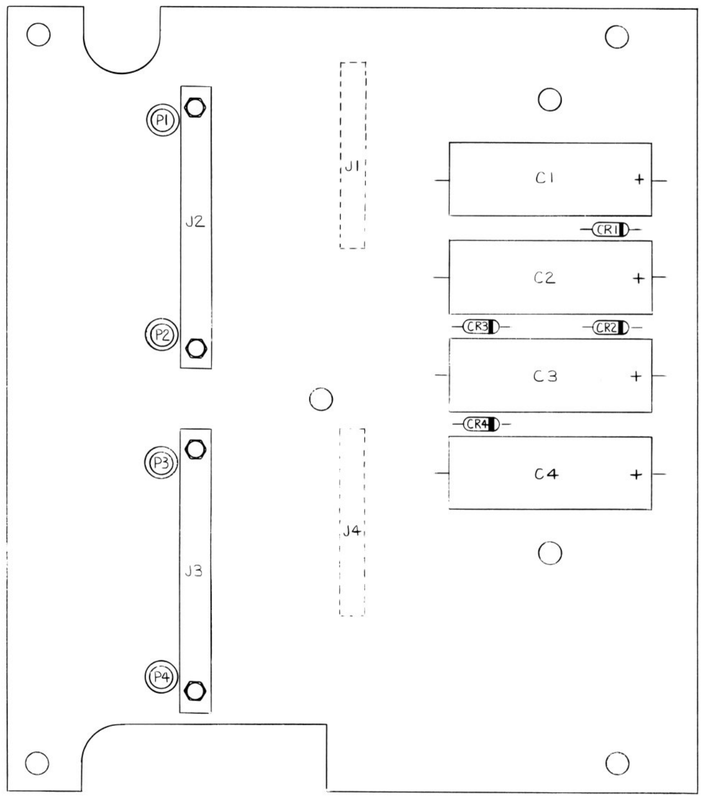


Figure 6-7. A7 I/O Module (Main) PCA (cont)



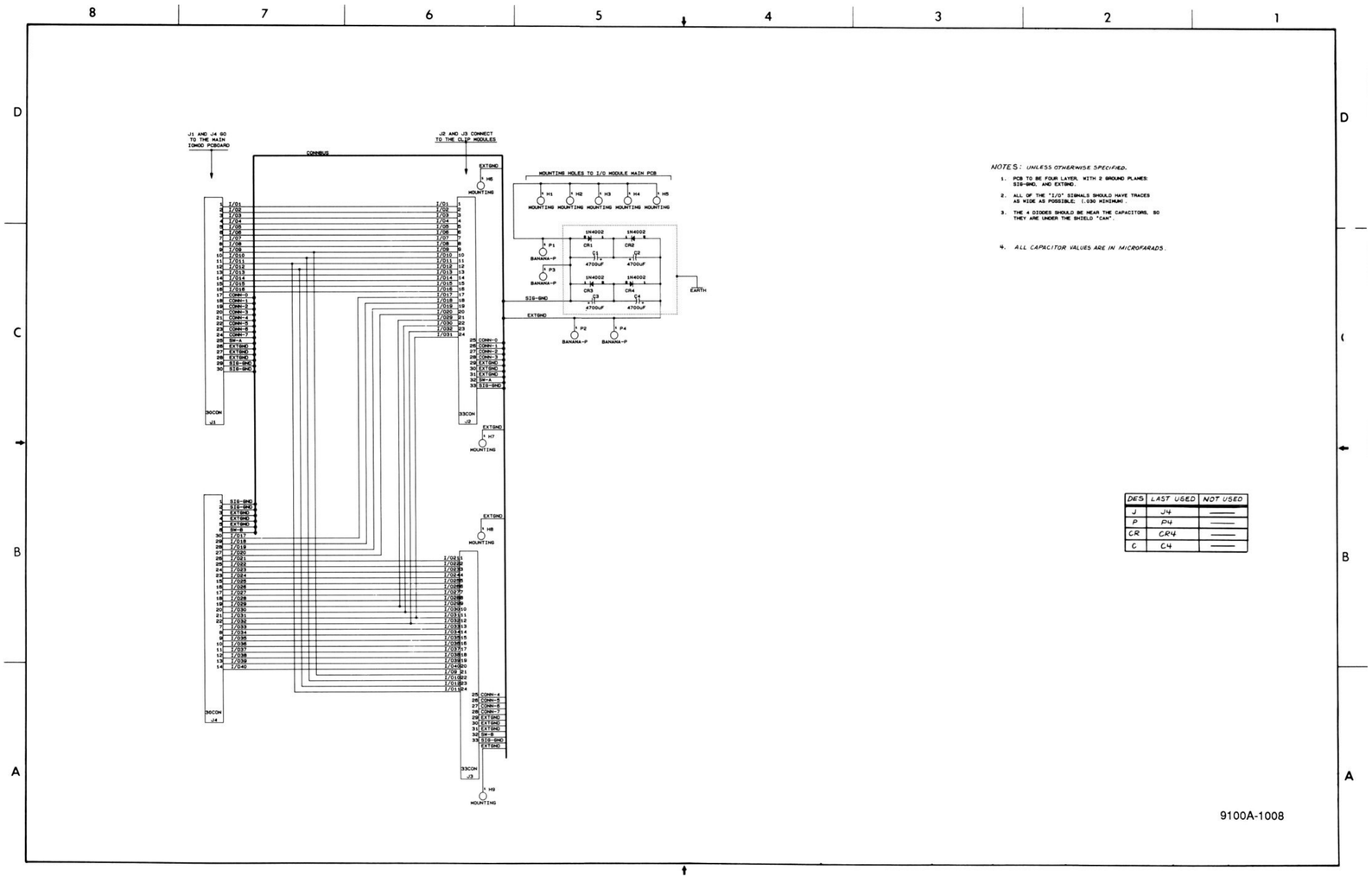
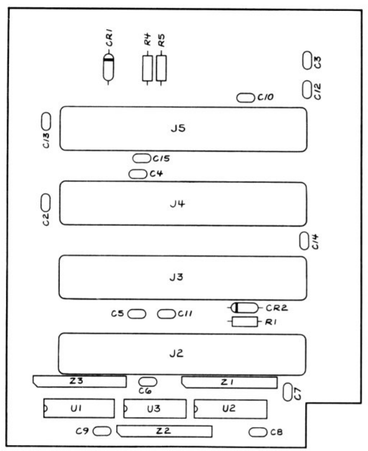
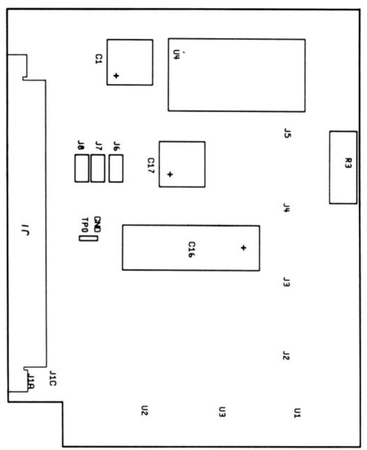


Figure 6-8. A8 I/O Module (Top) PCA

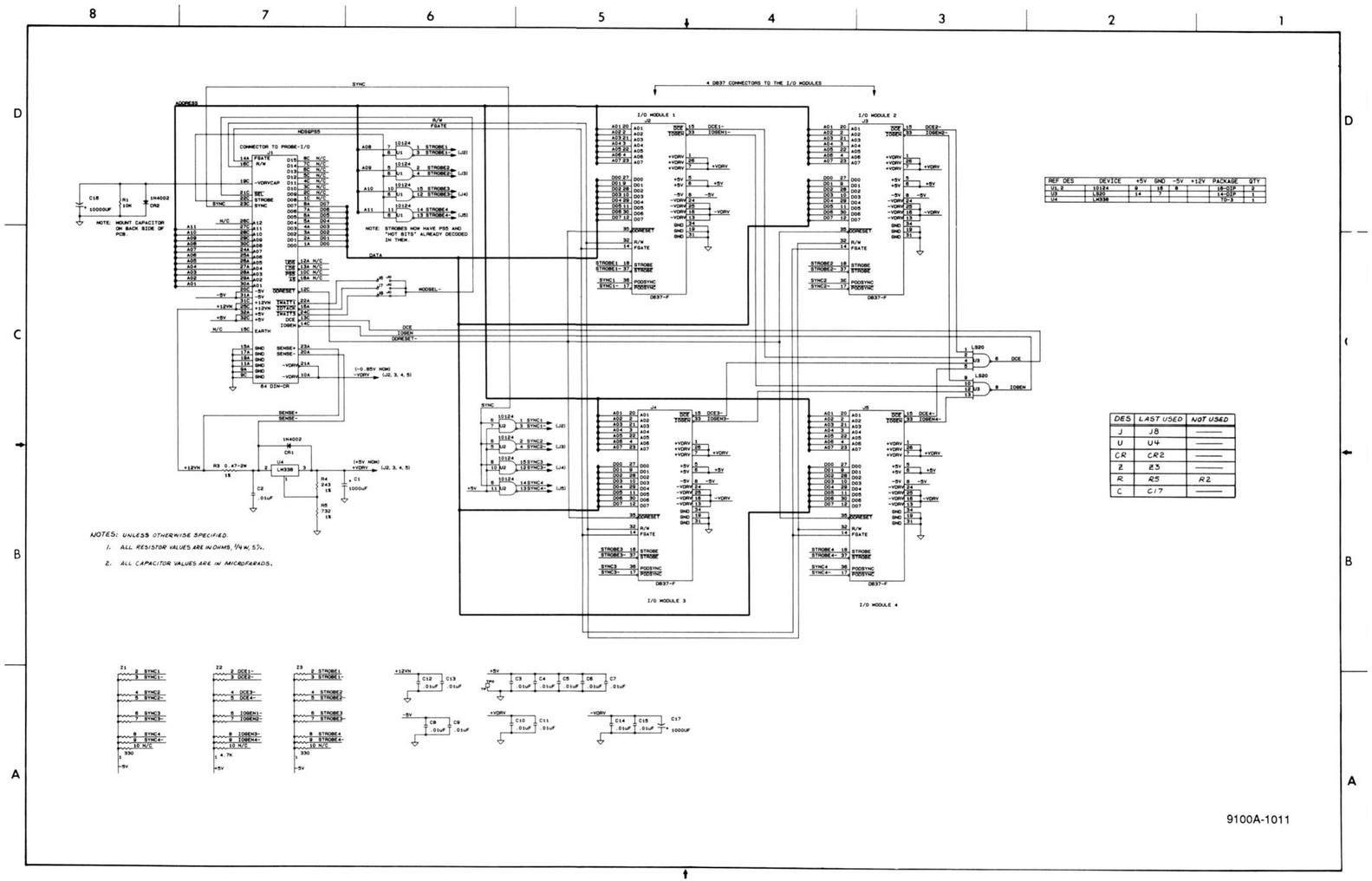


CKT 4 SIDE



CKT 1 SIDE

9100A-1611



REF DES	DEVICE	+5V	GND	-5V	+12V	PACKAGE	QTY
U1,2	10124	8	16	8		16-DIP	2
U3	LS20	14	7			14-DIP	1
U4	LM339				12-3	1

DES	LAST USED	NOT USED
J	J8	
U	U4	
CR	CR2	
Z	Z3	
R	R5	R2
C	C17	

Figure 6-9. A11 I/O Connector PCA

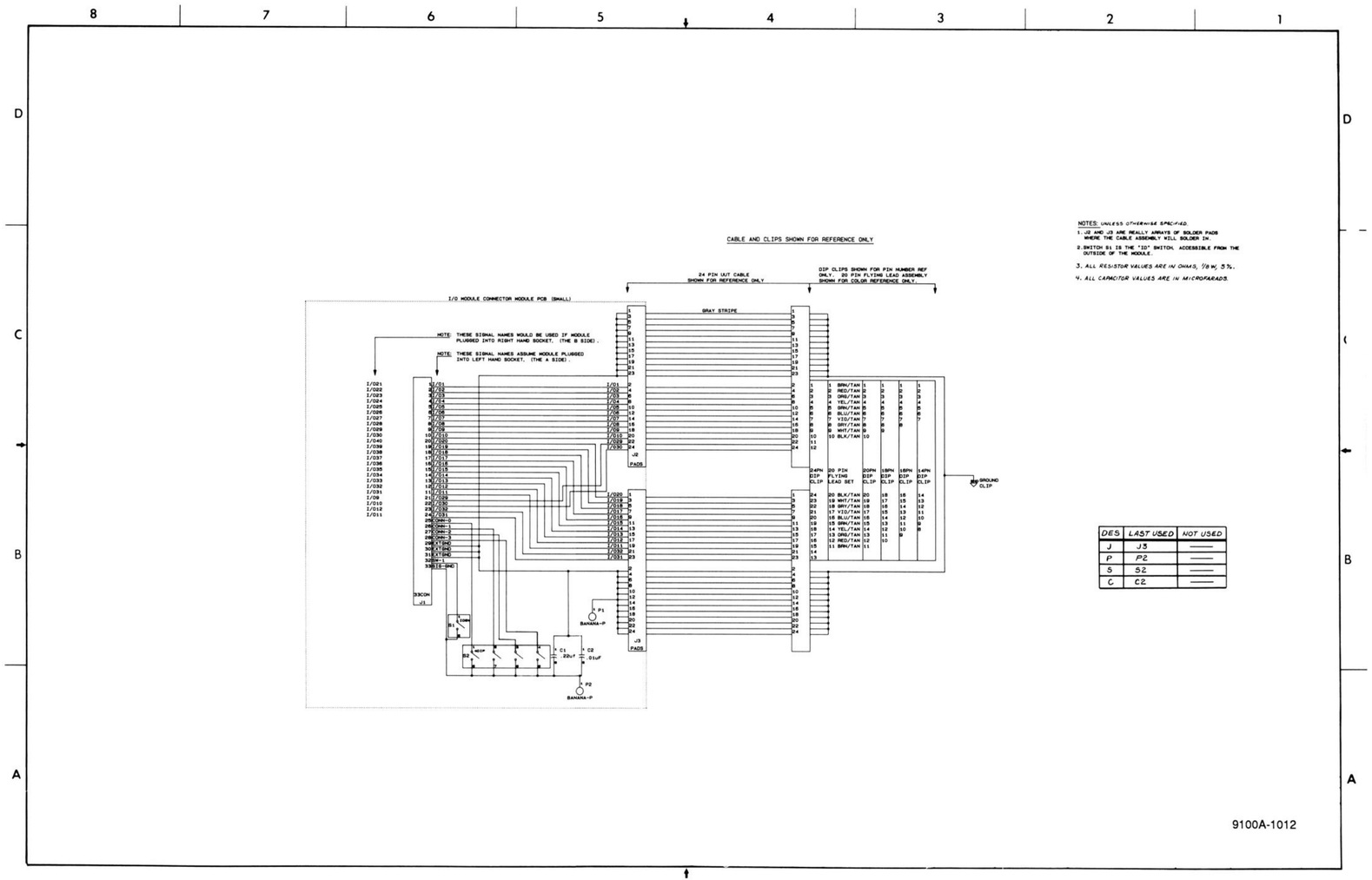


Figure 6-10. A12 DIP Clip Module (Half)

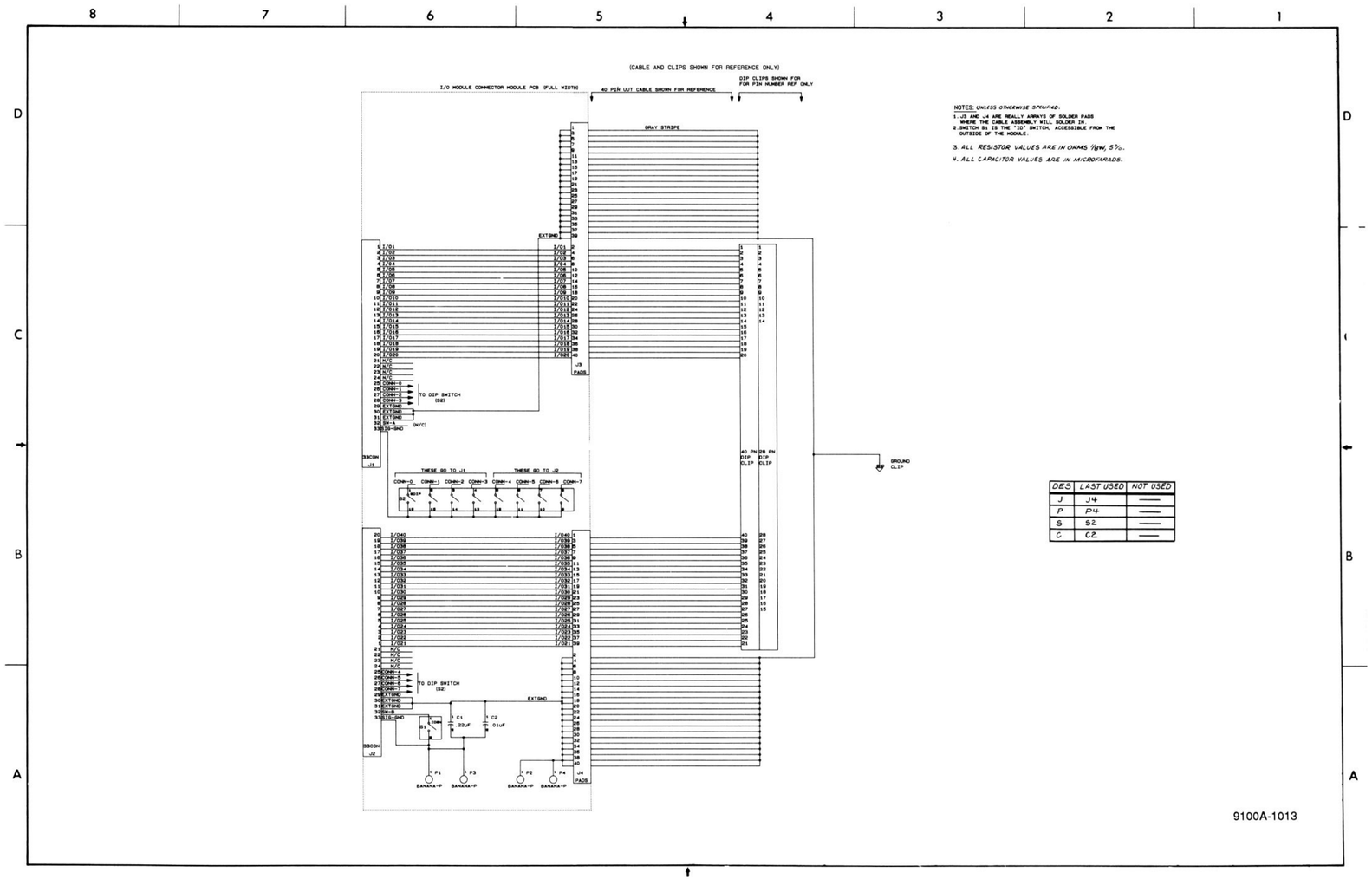


Figure 6-11. A13 DIP Clip Module (Full)

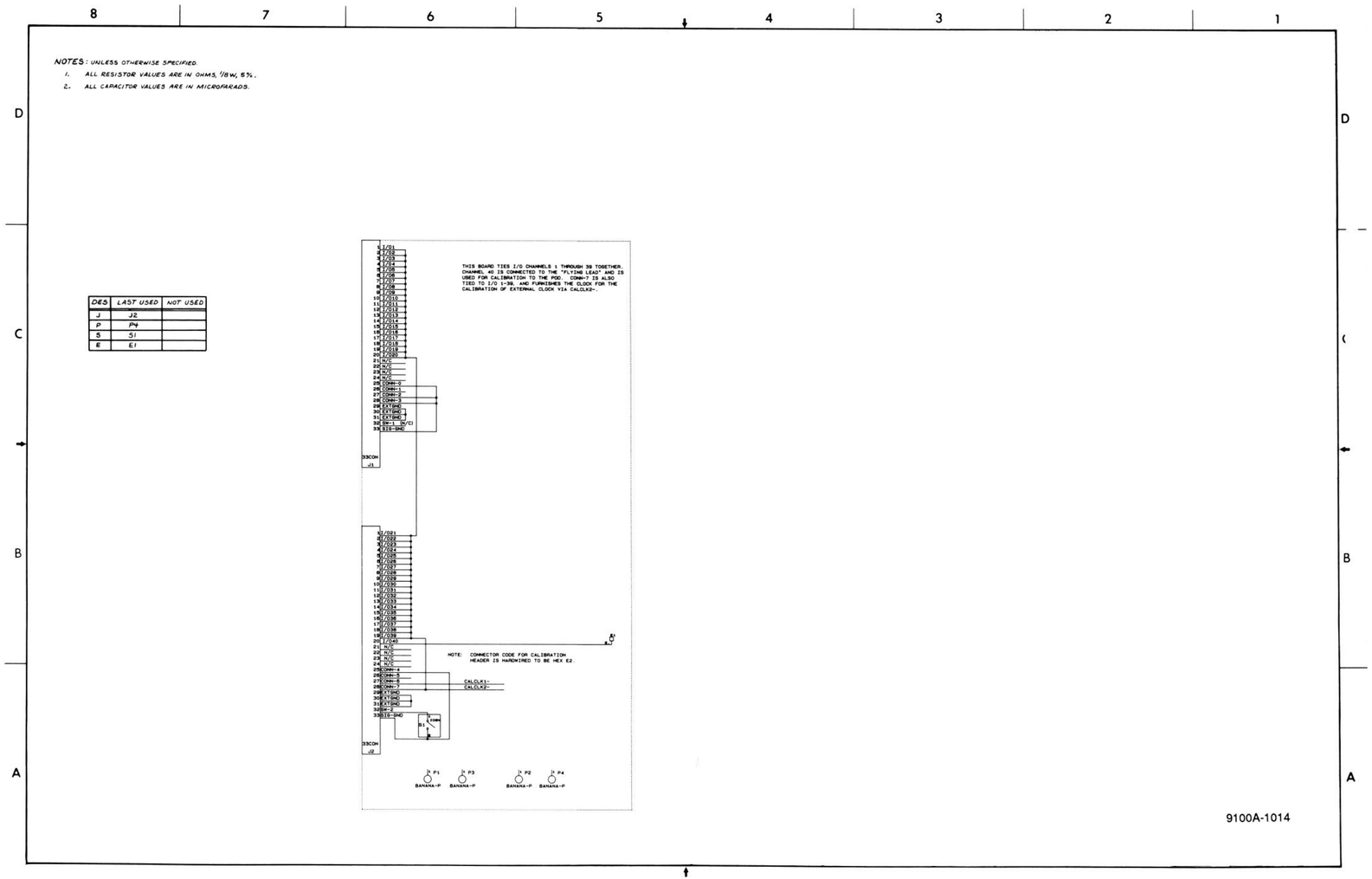


Figure 6-12. A14 Calibration Module PCA

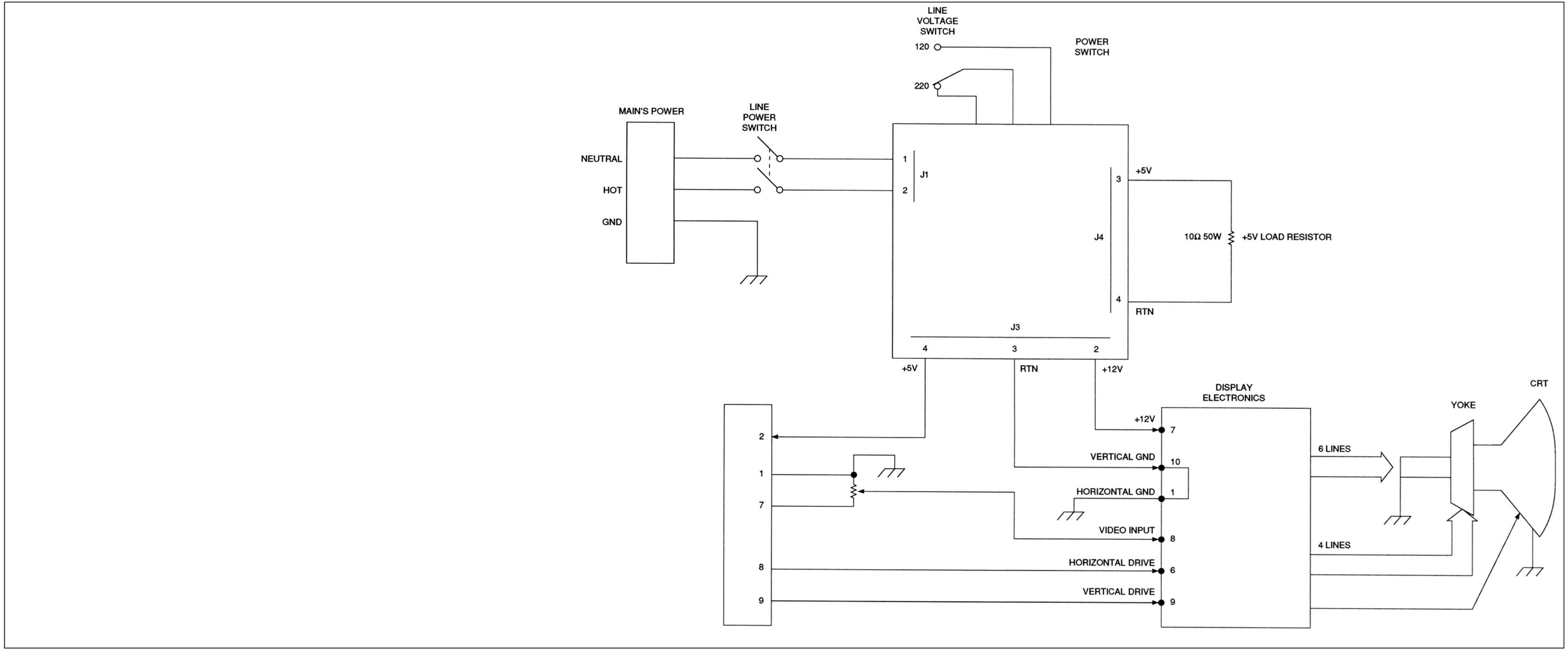
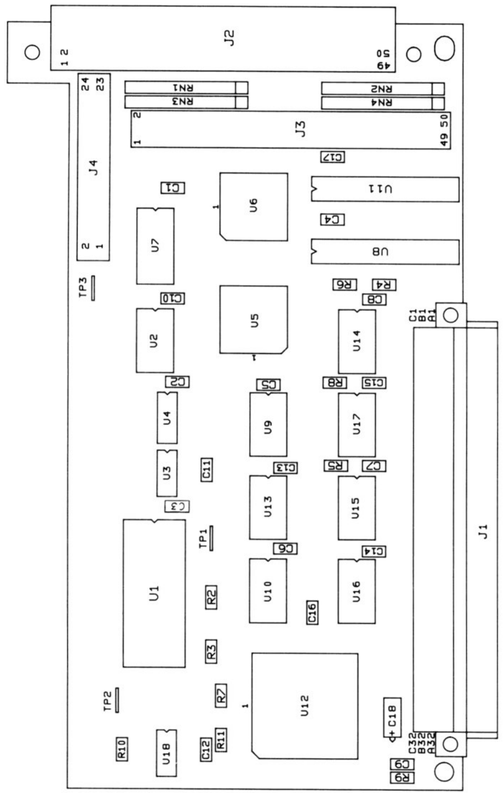


Figure 6-13. A19 Monochrome Monitor, Block Diagram



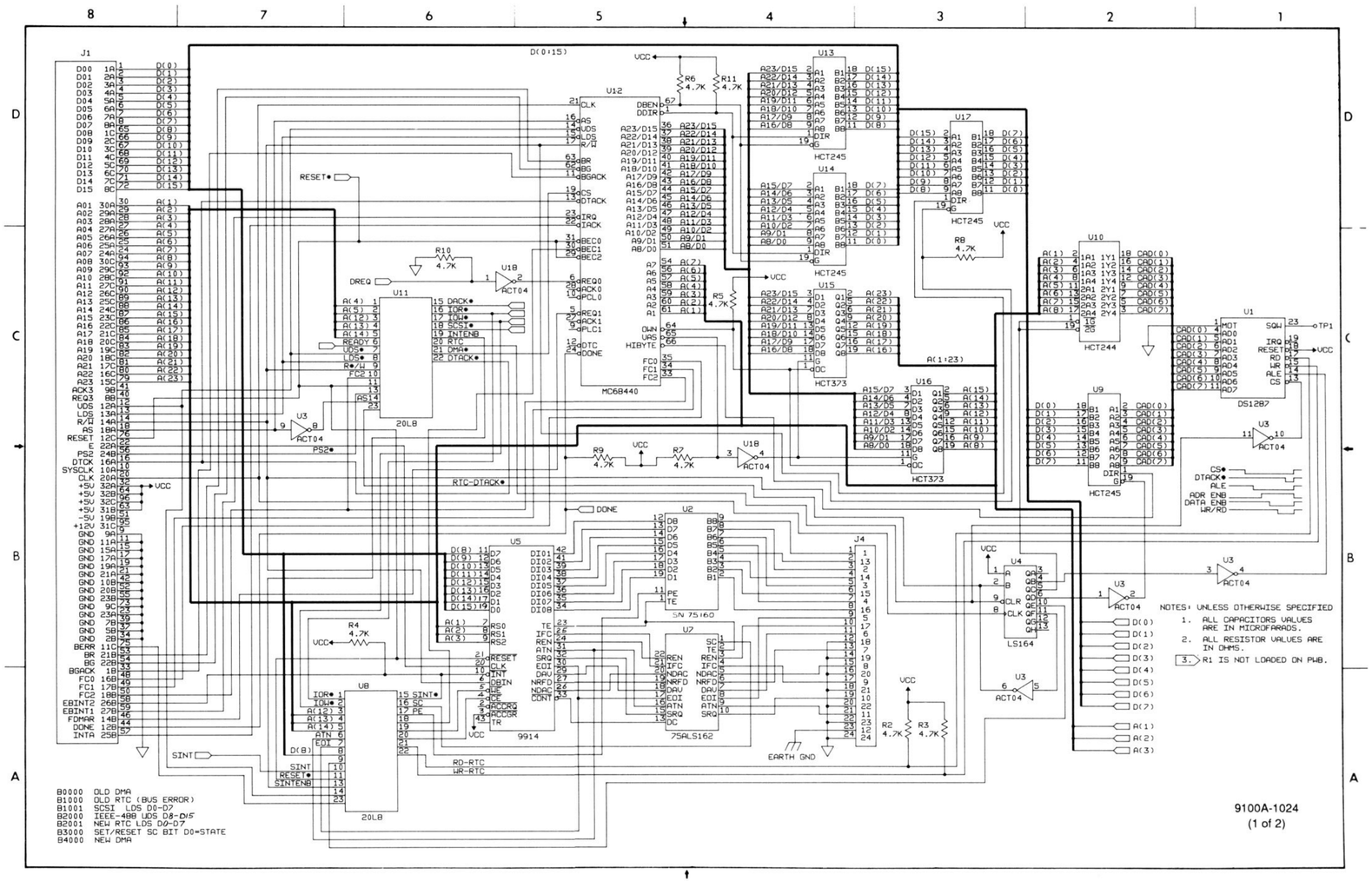
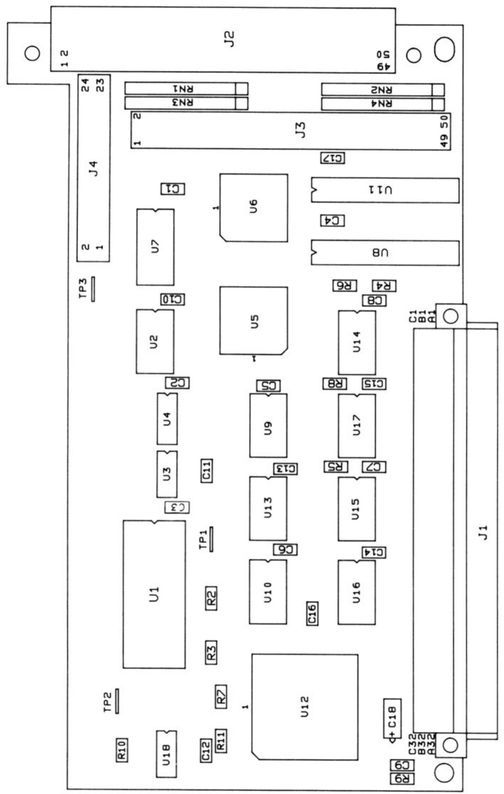
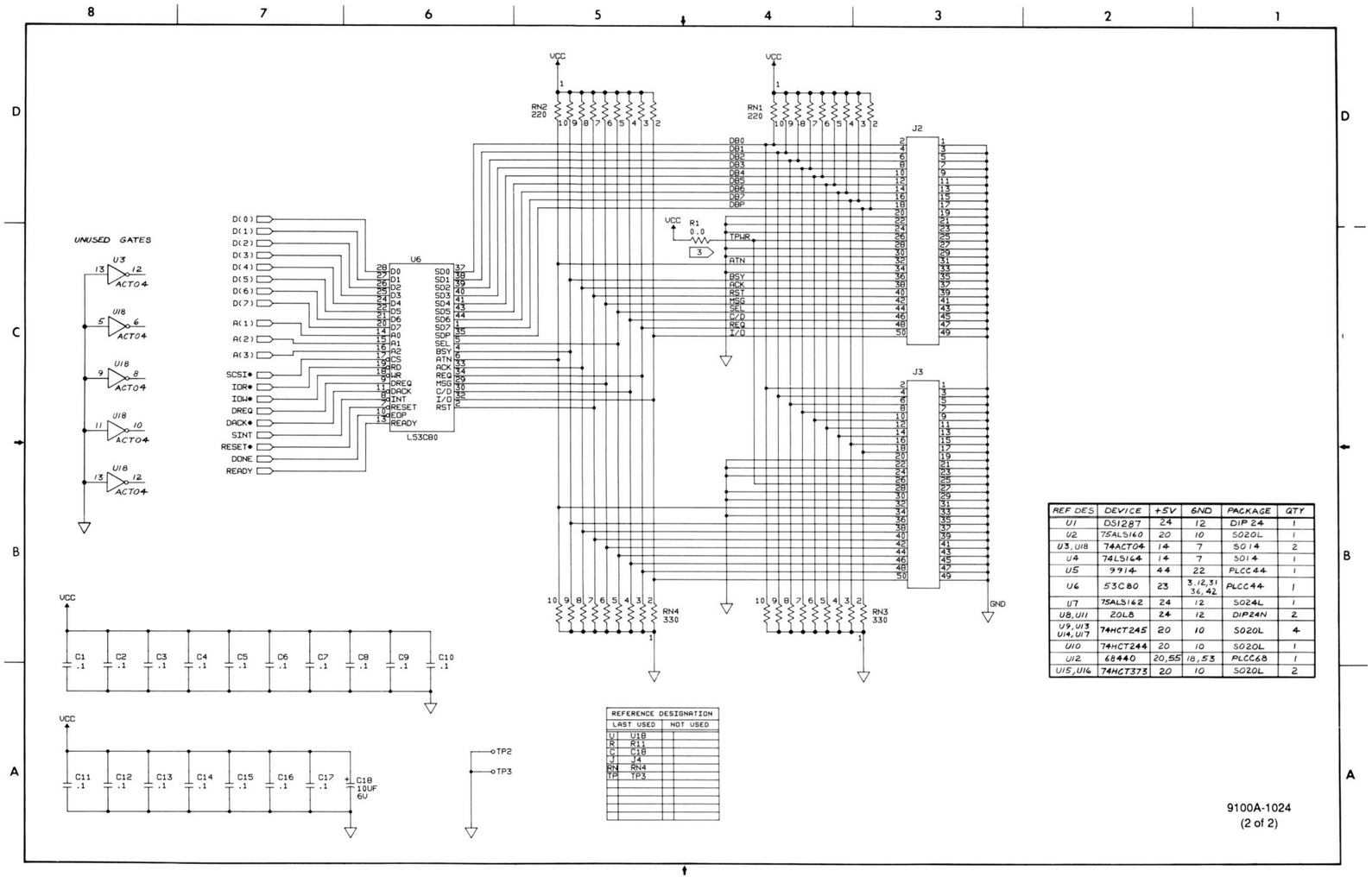


Figure 6-14. A24 Multi-Function Interface (MFA) II PCA





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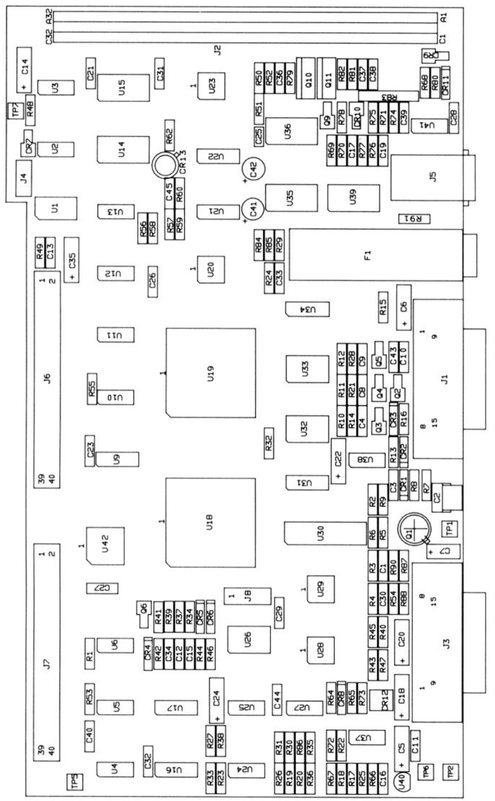
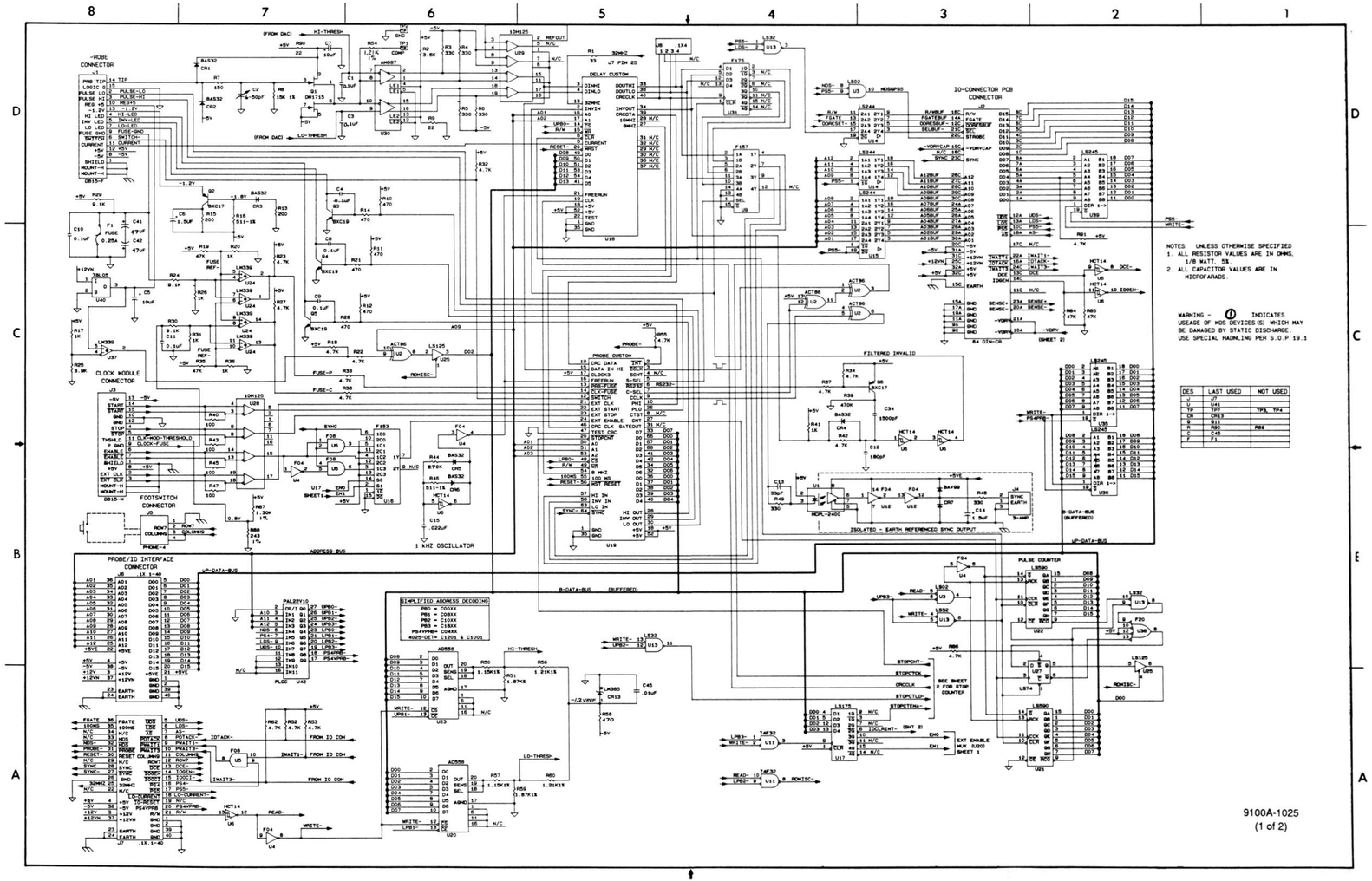
U2	75ALS160	20	10	SO20L	1
U3,U18	74ACT04	14	7	SO14	2
U4	74LS164	14	7	SO14	1
U5	9914	44	22	PLCC44	1
U6	53C80	23	3,12,31 36,42	PLCC44	1
U7	75ALS162	24	12	SO24L	1
U8,U11	20L8	24	12	DIP24N	2
U9,U13 U14,U17	74HCT245	20	10	SO20L	4
U10	74HCT244	20	10	SO20L	1
U12	68440	20,55	18,53	PLCC68	1
U15,U16	74HCT373	20	10	SO20L	2

Figure 6-14. A24 Multi-Function Interface (MFA) II PCA (cont)

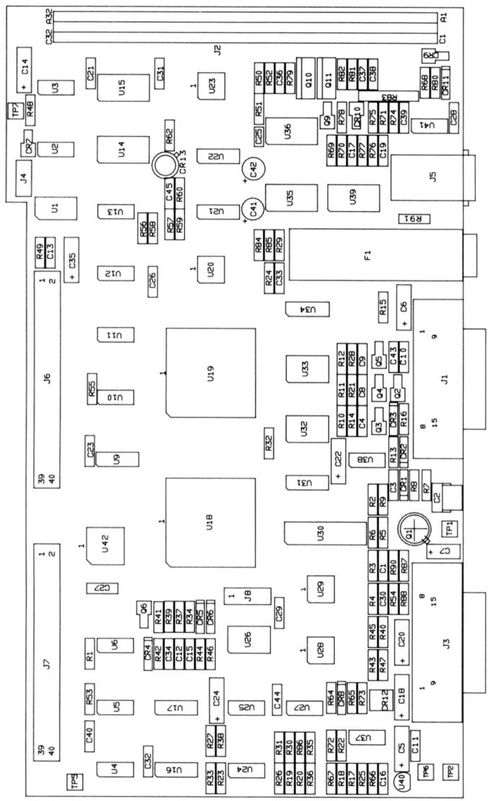


9100A-1625



9100A-1025
(1 of 2)

Figure 6-15. A25 Probe I/O-ECL PCA



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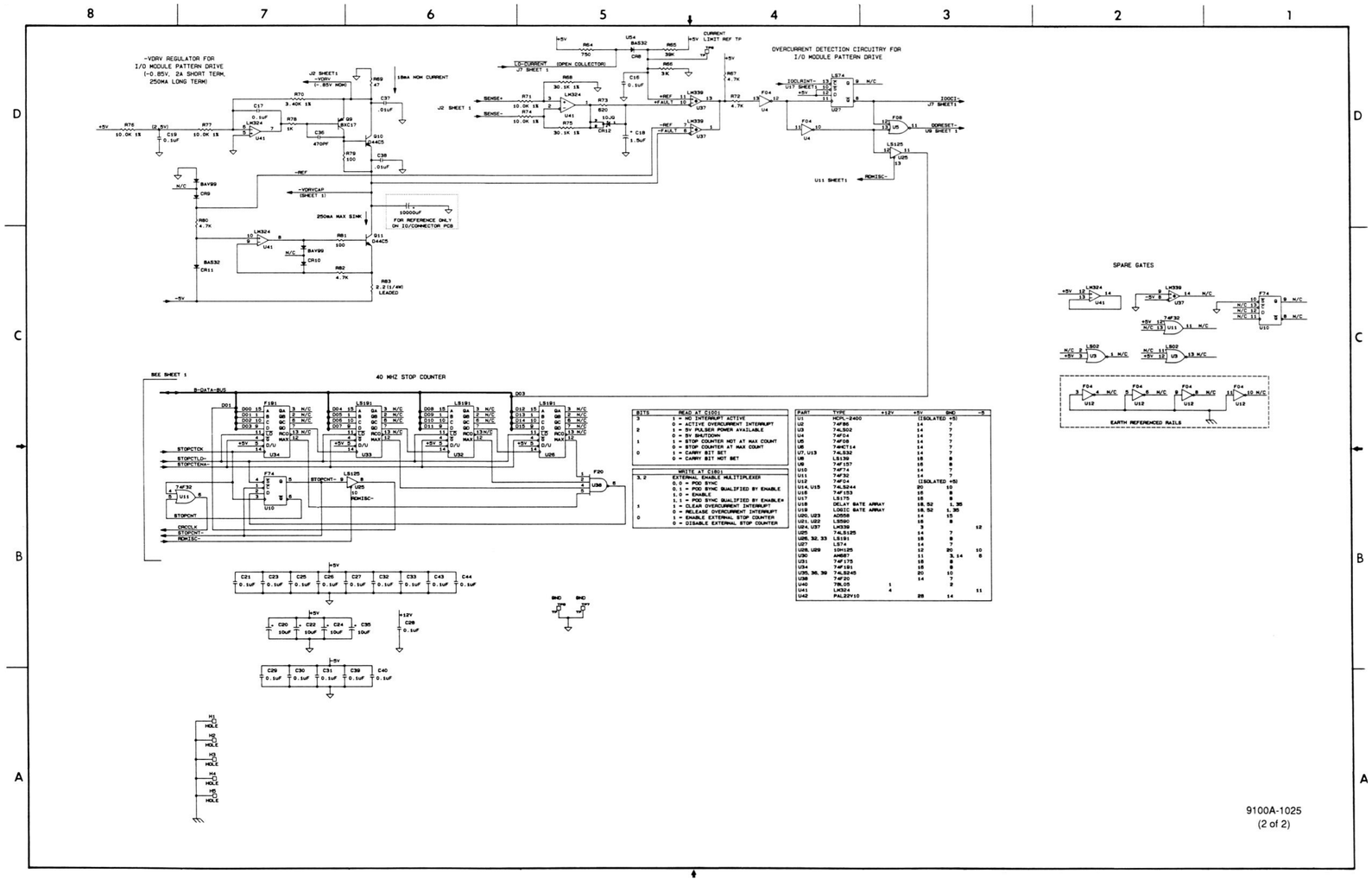

Figure 6-15. A25 Probe I/O-ECL PCA (cont)

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